ОБЪЕДИНЕННЫЙ
ИНСТИТУТ
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ИССЛЕДОВАНИЙ

Дубна

E13 - 6856

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DIGITALLY CONTROLLED FAST LOGIC MODULES

1972

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Submitted to IEEE
Nuclear Science Symposium

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Introduction

The particular problem of the fast logic system operating with particle detectors is to eliminate the instability of the inherent delay in every logic channel and to control this parameter during the period of the experiment. This is important when the logic channels contain such devices as photomultipliers, discriminators and logic circuits and the time resolution in the nanosecond and subnanosecond region is required. Automatic setting of the coincidence system makes easier also the adjustment of other parameters as the amplification of photomultipliers, the threshold of discriminators, etc. This paper presents some results of a project of the fast coincidence system connected to the CAMAC autonomous control system.

At the present state of the project, the parameters controlled during the experiment were only the inherent delay of the logic channels and the operating mode of the coincidence unit. For the first purpose, the digital delay using the hybrid integrated circuits - diode switches and dual diode switches - was developed. For the second purpose, the emitter coupled logic circuit following the modified MECL III integrated circuit philosophy was developed. The delay unit and the coincidence unit were digitized using the CAMAC interface. The diode switches and the dual diode switches can be used in digital attenuators possessing very important features. The use of digital attenuators allows to extend the range of the digitally controlled parameters of the counter system.

System Description

Figure 1 shows the digitally controlled fast logic system. As indicated, the counters - the scintillators and the photomultipliers - are connected via digital delays with the digital coincidence unit. The particle beam passing through the counters defines the time intervals at which the counters are triggered. The triggering time intervals are simulated by the delays inserted between the respective gallium phosphide light diodes and the common output of the pulse generator. The delays are set manually. The digital delays, the digital coincidence unit, and the scaler are connected via the dataway with the control units. The CAMAC compatibility rules were followed in the system. The control cycle for the automatic setting of the coincidence system will be described below.

The CAMAC interface used for both the digital delay and the coincidence unit is shown in Fig. 2. It contains the 5-bit digital module register which can be loaded in a normal command cycle. The command functions are Read, Write, Clear, Increment, and Enable used for manual setting of the register. In the digital dealy unit, the 5-bit register used for the delay control is referred to as the delay register. The delay register permits to increment the delay in 32 equal steps. In the digital coincidence unit the digital module register used for the operating mode control is referred to as the operating mode register. The operating mode register permits the coincidence operation of any two, three, or four selected channels by applying the ''0'' logic level to their NOR gates and the ''1'' logic level to the other NOR gates (Fig. 1).

The coincidence system has four logic channels numbered from 1 to 4, which are used in the normal coincidence mode of operation during the experiment. The reference ''Zero'' channel is used during the control cycle for generating the reference timing signal. During the period of experiment the ''Zero'' channel can be used in both the coincidence and the anticoincidence mode of operation.

Digital Modules

1. Digital Delay

The design of a digital delay performing the transfer of fast analog signals and not only logic signals became possible due to the

development and availability of the $p-i-n$ diodes and $p-n$ switching diodes in recent years [1]. The important characteristics of these diodes are the very low diode resistance of the order of 10^{-1} ohms when, for instance, the direct current of 8 mA flows through the diode in the forward direction, and the small capacitance of the order of 10^{-1} pF when the diode is biased in the reverse direction. Using these diodes, the basic circuit - the diode switch - was designed as the hybrid integrated circuit composed of less expensive $p-n$ switching diodes. The diode switches and the dual diode switches can be used in digital delays, as well as in digital attenuators, even in digital diode switches themselves. The important characteristic of the diode switch is the low and constant attenuation $<$ 0.5 dB for the wide dynamic range of input pulses (±100 V) in the switch-on state. Its disadvantage is a rather small switching-off time constant, of the order of 100 ns, for the step-function pulse applied to the input. This limits the use of diode switches to transferring only fast signals or very short pulses. Better results can be achieved using the $p-i-n$ diodes in the switches. Another disadvantage of the diode switch is the small range of signal d.c. component, which it can transfer without appearance of limiting effects and pulse shape distortion. Therefore, in digital delays, the d.c. component transfer is desirable to be rejected.

The block diagram of the digital delay is shown in Fig. 3. The diode switches and the dual diode switches are shown schematically; the solid lines indicate the forward biased diodes with very low diode resistance, the thin lines indicate the diodes in zero bias state. The characteristics of the digital delay: the delay can be varied in 32 steps; the minimum delay is 3 ns; the delay increment is 0.25 ns. The total attenuation is 5 dB, the feedthrough is smaller than 60 dB, the output pulse risetime is 1.2 ns. Both the last characteristics were measured for an input pulse risetime of 0.6 ns. The circuit diagram of the first bit of the digital delay is shown in Fig. 4. The ferrite inductances are 100 μH.

2. Digital Coincidence Unit

The digital coincidence unit has the input and output circuits compatible with NIM standard logic levels. Inside the unit, the positive emitter coupled logic is used with the logic levels 0V and +1V. The unit can operate at pulse repetition rates of 200 MHz and

the logic pulses are generated with the rise- and falltimes of approximately 1 ns and pulse width smaller than 2 ns. All the logic is d.c. coupled and the basic OR-NOR gate is used with complementary signals for AND-NAND operation. The following basic submodules are used in the coincidence unit shown in Fig. 1.

The fixed threshold discriminators D1-D4 are intended for the front-edge timing of scintillation pulses. The circuit diagram of the discriminator is shown in Fig. 5. The input limiter and differentiator described in [2,3] were used for their good fast response characteristics. The tunnel diode discriminator was developed to increase both the maximum triggering rate and the sensitivity . The fixed threshold discriminator can be triggered at pulse repetition rate of 300 MHz keeping the sensitivity of 100 mV.

The 3-input OR-NOR gate circuit diagram is shown in Fig. 6. The discrete transistors were used with f_T = 1.5 GHz. The pulse pair resolution of 4 ns was achieved.

The fast trigger circuit T0-T5 shown in Fig. 7 links the tunnel diode discriminator with the two-input OR gate. Both inputs are used to inhibit trigger operation. The trigger circuit generates logic pulses with the rise- and falltimes of approximately 1 ns. The triggering rate larger than 300 MHz was obtained.

The NIM to the emitter coupled logic input circuit and the emitter coupled logic to the NIM output circuit are shown in Fig. 8 and Fig. 9. They complete the digital coincidence unit circuitry.

Control System

The control cycle can be performed during the period of experiment. The scan programme is started by selecting the reference channel and one of the logic channels in coincidence. The digital delay is incremented in steps and at every step the code of 128 timing pulses is generated by the light diodes. The scaler at the output of the coincidence unit counts the coincident pulses. The data from the scaler is transferred to the data register of the programming unit (Fig. 10). The number comparator informs whether the number of counts is larger than 64, that is whether the true coincidences were registered. The scan logic specifies the addition or subtraction mode in which the scan register and the subtraction register are to be incremented. The subtraction register counts the half of the

number of the steps during which the true coincidences were registered. Fig. 11 shows the delayed coincidence curve together with the scanning scheme. The scan register is being incremented in the addition mode while the true coincidences are registered. If for more than two steps the true coincidences were not registered, Flag 1 is generated and the scan register and the subtraction register are incremented in the subtraction mode unless the subtraction register is cleared. Then Flag 2 is generated and the next channel can be scanned. Fig. 12 shows the programme flow chart of the control cycle.

The number of the code timing pulses, the level of the number comparator and Flag 1 were indicated as an example. They are to be discussed in specific experimental conditions individually.

This work is considered to be a little contribution to the efforts in designing the CAMAC modules of specific interest.

The author would like to thank Dr. S.V.Mukhin's experimental team from the Laboratory of High Energies for the permanent support, which has made this work possible.

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Received by Publishing Department
on December 22, 1972.

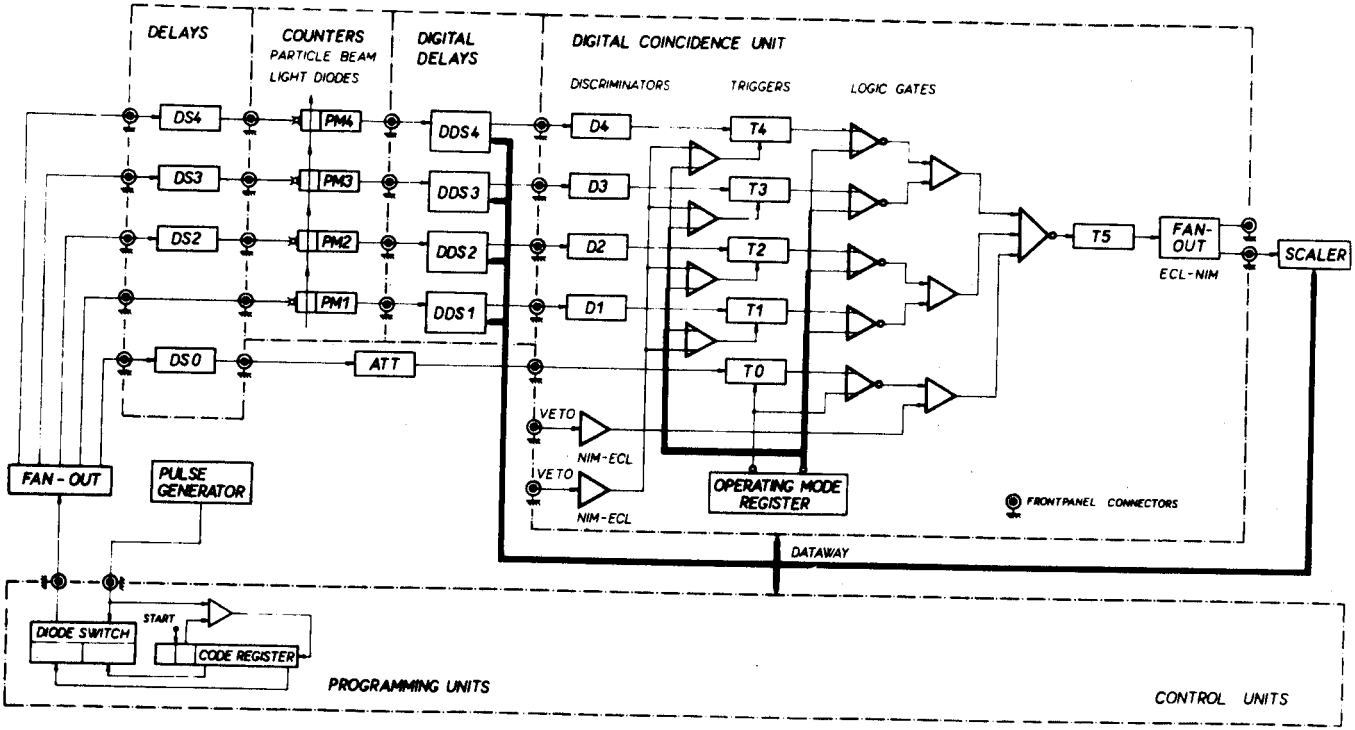


Fig. 1. The block diagram of the fast coincidence system.

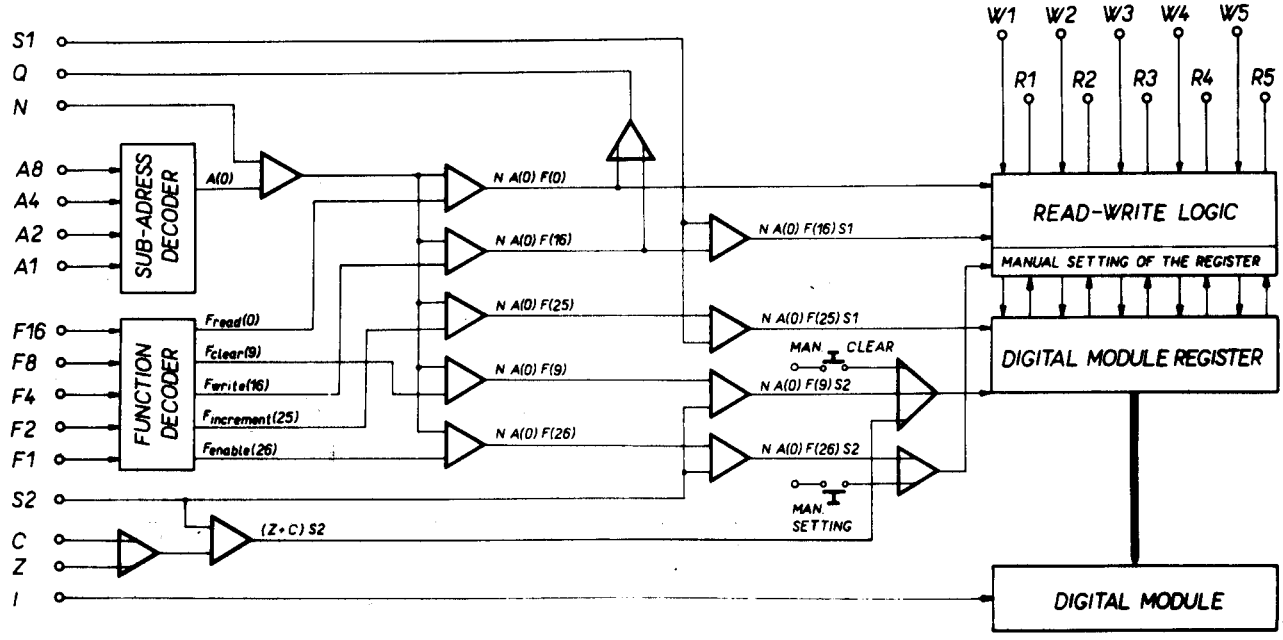


Fig. 2. The CAMAC interface for the digital logic module.

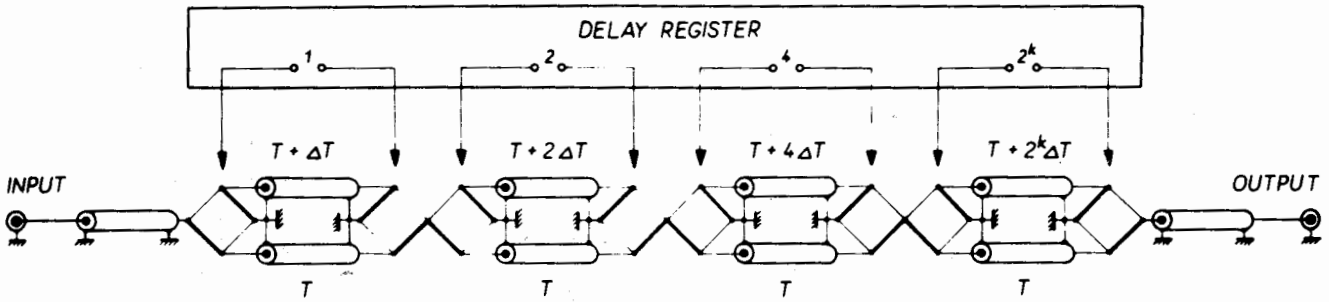


Fig. 3. The block diagram of the digital delay.

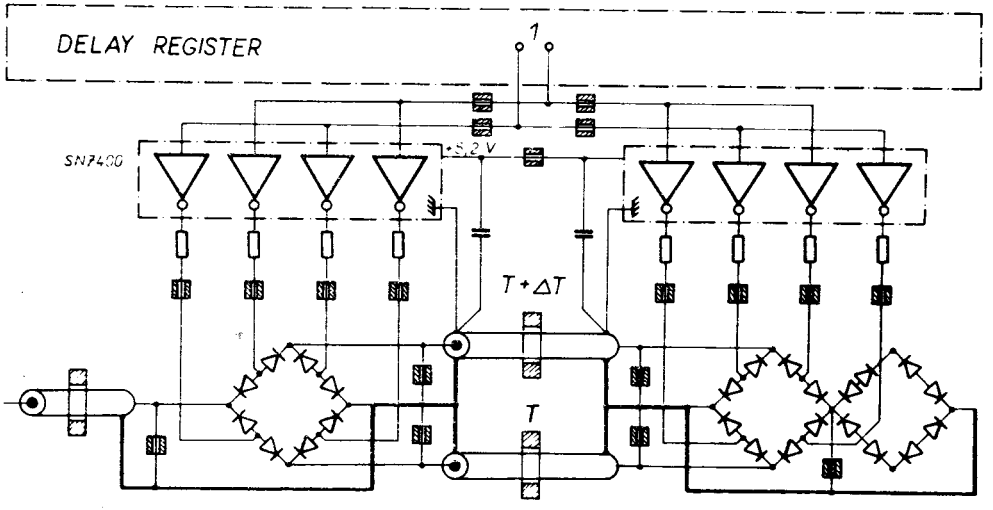


Fig. 4. The circuit diagram of the first bit of the digital delay.

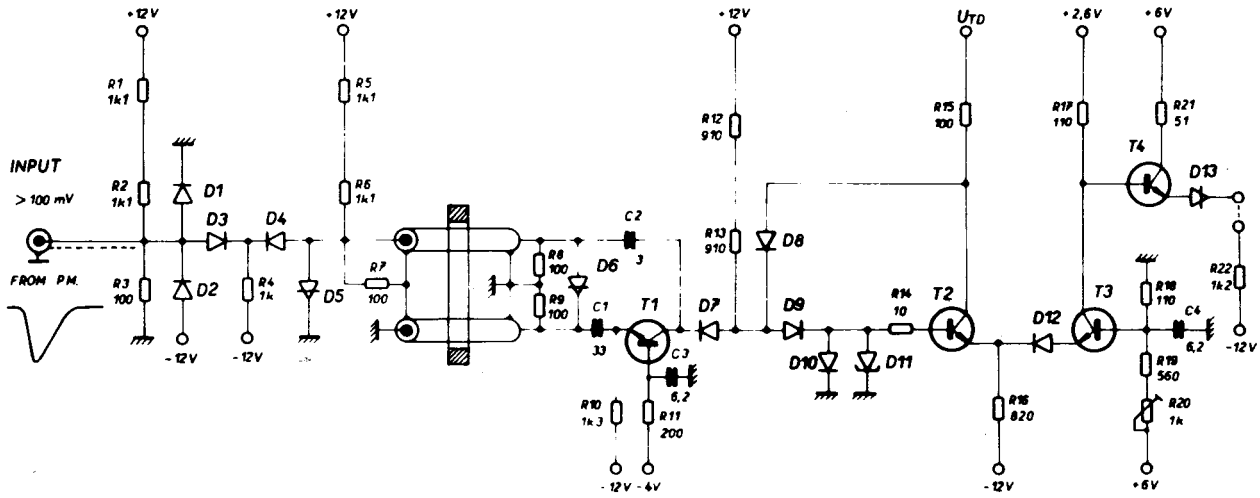
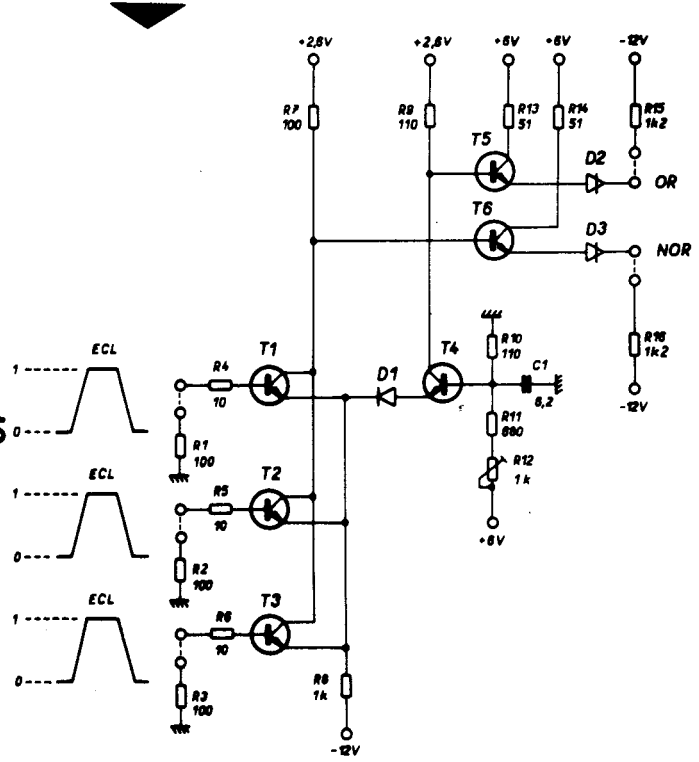


Fig. 5. The fixed threshold discriminator. Note: T1-T4: 1T330G; D1, D2: KD503B; D3, D4, D7-D10, D12: 1D508A; D5, D6: GI403A; D11: AI201A; D13: AI402E.

Fig. 6. The 3-input OR-NOR gate. Note: T1-T6: 1T330G; D1: 1D508A; D2, D3: AI402E.



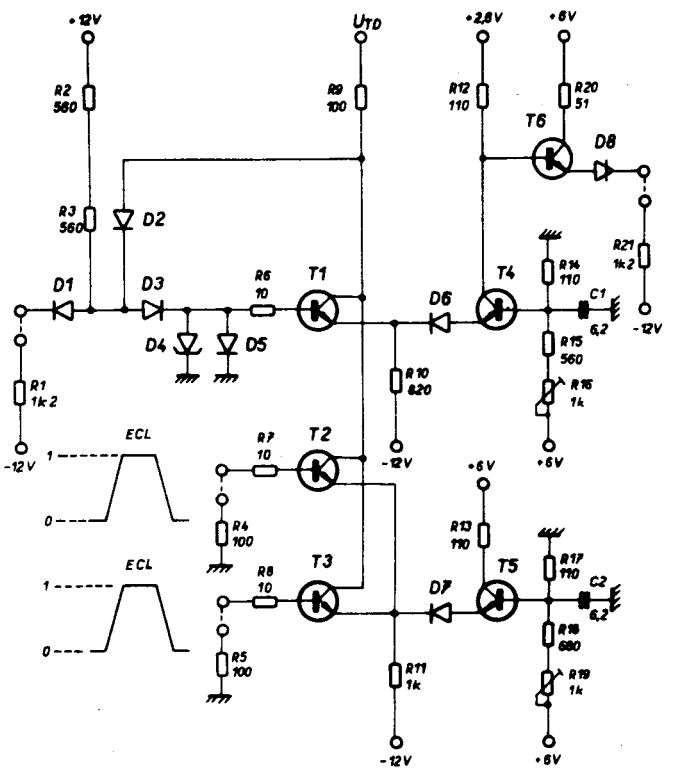


Fig. 7. The fast trigger circuit. Note: T1-T6: 1T330G; D1-D3, D5-D7: 1D508A; D4: AI201A; D8: AI402E.

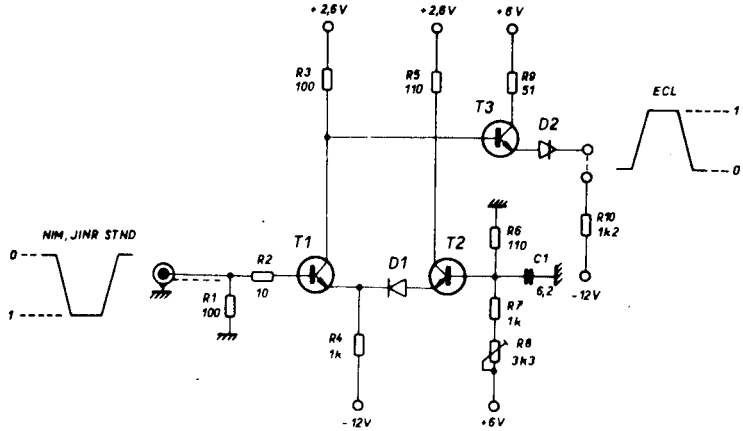


Fig. 8. The NIM to the Emitter Coupled Logic input circuit. Note: T1-T3: 1T330G; D1: 1D508A; D2: AI402E.

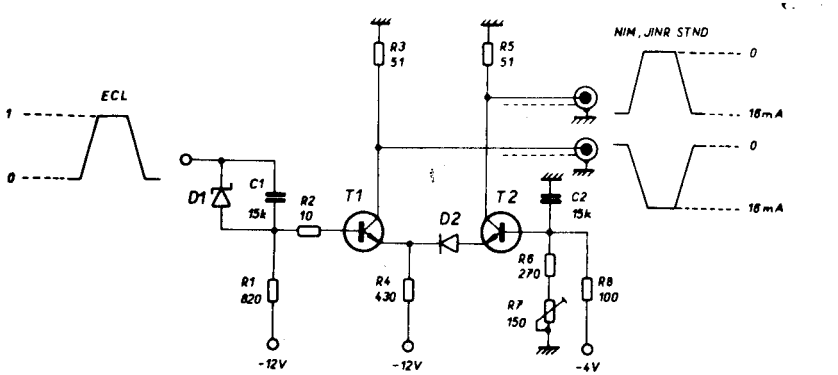


Fig. 9. The Emitter Coupled Logic to the NIM output circuit. Note: T1, T2: 1T330G, D1: KS139A; D2: 1D508A.

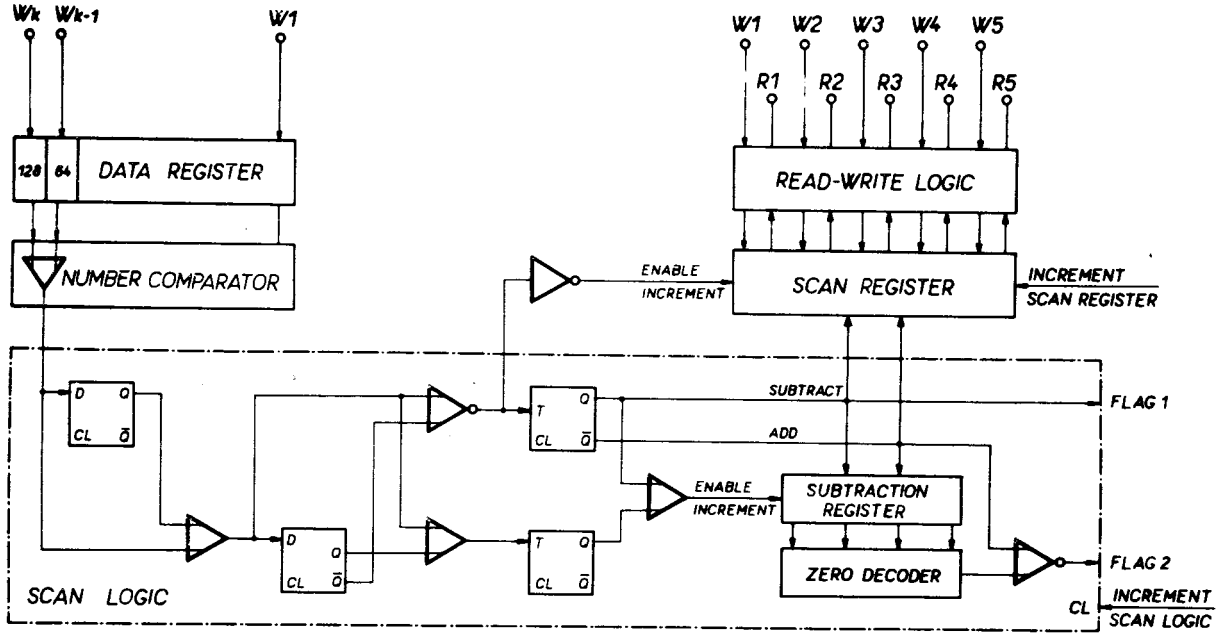


Fig. 10. The scan logic.

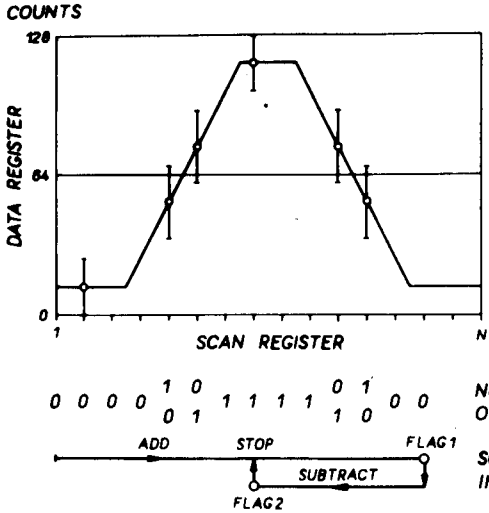


Fig. 11. The Delayed Coincidence curve and the scanning scheme.

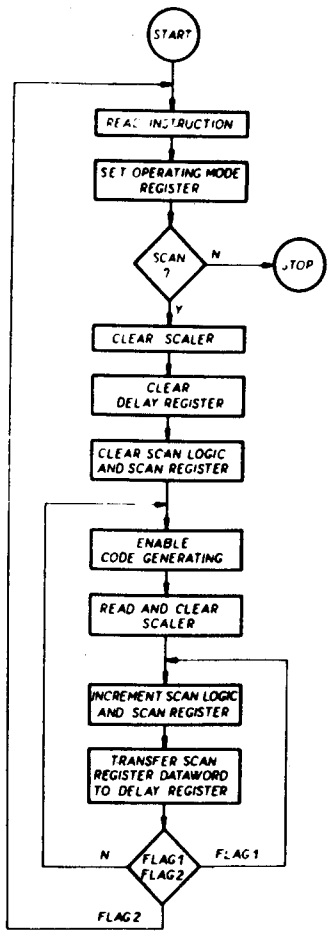


Fig. 12. The programme flow chart of the control cycle.