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# FAST DISCRIMINATORS

ЛАБОРАТОРИЯ ЯДЕРНЫХ ПРОБЛЕМ

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# FAST DISCRIMINATORS



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*Introduction*

The high counting rates of scintillators and fast photomultipliers used in an electronic system for the measurement in high energy physics experiments has increased the performance demanded from logic modules, including fast discriminators. The particular problem in designing fast discriminators is concerned with providing a suitable dynamic range of input pulse amplitudes and very high counting rates, as well as the long time stability of output timing pulses. The importance of very high counting rates and high signal resolution has increased when the large accelerators have started to operate in the last few years. In order to ensure the minimum "true events" count-losses in the electronic logic system, the following specifications of fast discriminators would be desirable:

Triggering rate: 200 MHz

Input signal resolution: $\leq$ 5 ns

Output pulse pair resolution: $\leq$ 5 ns

Dynamic range of input pulse amplitudes: 52 dB

Long time stability of output timing pulses during the experiment run: $\pm$ 10 ps

Time resolution of the AND operation: $\leq$ 1 ns

To approach the above mentioned requirements, the attempts were made to use new principles and circuits in fast discriminators: The fast input limiter and differentiator [2,4], has the potential of limitation and differentiation input pulses of the pulse width spectrum in nanosecond and subnanosecond range. The p-i-n diode attenuator-invertor has the potential of continuously variable attenuation of signals with corresponding frequency spectrum from several megahertzes to several gigahertzes [5] . The subnanosecond logic output generator together with the temperature compensation circuits gives the possibility to fast discriminators to generate timing pulses of the $10^{-10}$ s pulse width, and the long time stability of timing pulses of the order of $10^{-11}$s.

The fast discriminators have been designed for front-edge timing and for amplitude selection of photomultiplier pulses. This paper contains description and more complete documentation of the following fast discriminators: the fixed threshold discriminator Model 5NS, the fixed threshold discriminator Model CT, the integral discriminator Model 5NS, and the differential discriminator Model 5NS or Model 5NS-CT.

*Design Considerations*

The modules are made up of a number of simple basic circuits, submodules. The function of each submodule within the fast discriminator modules is indicated in Fig.1. Each submodule could be operated individually and thus the versatility in designing discriminators was achieved. Since the basic submodules in various discriminators are identical, the circuit description will be concerned only with the individual submodules. Technical parameters will be presented for the complete fast discriminator modules.

The mechanical design of the modules employes the Vishnya standard. Inside one module with the 160 x 160 mm$^2$ frontpanel were inserted the Quad Discriminator, the Dual Discriminator plus Dual Integral Discriminator and the Differential Discriminator. The advantage of the rather large dimension of modules is in good temperature conditions, all four discriminators are being working at the same temperature and no forced air cooling is necessary.

In every discriminator the INPUT, the VETO and three of the nanosecond logic outputs N-LO are laid out to the frontpannel connectors. BNC connectors are used. One of the N-LO or the SN-O subnanosecond output can be used inside the module, for instance for AND or OR operation.

Printed board circuits are etched on one side of the board only, the other side is left as the solid ground plane.

The supply voltages required by the modules are in general $\pm$ 12 V. The other voltages + 8V/1A, -4 V/0.3A, +4.85 V/0.1A are being derived inside the modules by voltage stabilizers.

*Submodules Description*

1.Fast input limiter and differentiator Model 5 NS

The circuit diagram is shown in Fig.2. In the limiter circuit, the circuit consisting of the diodes D1 - D6, and the asymmetric-symmetric transformer is used. This circuit has been derived from a symmetric limiter, described in [2]. In difference with circuits described previously [1,3] no transistors are used in this limiter and thus the better efficiency of limitation, the wider dynamic range of input pulse amplitudes and higher rate of operation was achieved. The differentiation is obtained by the differentiating RC circuit, consisting of the capacitor C1 and of the input impedance of the common base transistor T1. The resistor R7 and the capacitor C2 are balancing elements, balancing the output of the differentiating circuit, with respect to the asymmetric connection of the differentiating circuit to the limiter.

## 2. Tunnel diode discriminator

The circuit diagram is shown in Figs.2,3. The tunnel diode discriminator consists of the diodes DI-D4. The tunnel diode D3 is operated in the monostable mode, generating pulse of 2 ns width.

## 3. Output pulse generator and the fan-out Model 5 NS

The circuit diagram is shown in Fig.3. This submodule consists of the monostable tunnel diode trigger DI, D2, the circuit for tunnel diode current switching into two low impedance branches with a defined delay difference D3 - D5, the adding circuit T2, T3, the output fan-out circuit T4 - TI0, and the VETO circuit TI. The monostable tunnel diode trigger generates pulses of I ns width. The switching and the adding circuit makes the output pulse generator deadtimeless by adding the tunnel diode trigger pulse via 25 ohms delay line to the original pulse in the collector of T3. The fan-out delivers nanosecond logic outputs N-LO and the subnanosecond output SN-O. Two of N-LO are negative output pulses, one of N-LO is inverse logic output pulse.

The output pulse generator and the fan-out contain the temperature compensation circuits. The drift of tunnel diode DI bias current and the drift of currents of the associated elements D3 -D5, T2, T3 were temperature compensated by means of the resistor-thermistor divider RI, R2. The drift of the pulse amplitude of nanosecond logic output pulses was temperature compensated by means of the resistor-thermistor divider R3I-R33. The drift of the timing pulse of the subnanosecond output was temperature compensated by means of the resistor-thermistor divider R5I-R56. Temperature compensation of the tunnel diode bias current drift and timing pulse drift must be adjusted individually in every discriminator. Temperature compensation extends reliable performance of modules over the temperature range of I5-55$^{\circ}$ C.

The VETO circuit TI allows gating of the discriminator. The choice of a logic signal or inverse logic signal at the VETO input allows the anticoincidence or coincidence operation to be performed.

## 4. Input limiter and differentiator Model CT

The circuit diagram is shown in Fig.4. The limiter and differentiator has the individual stages functionally identical with the ones described in /1/ and differs only in some details. It consists of the following functional parts: the input diode current switch DI-D5, the transistor current switch TI, T2, the differentiator T3. The input limiter forms input signal and limits it to -200 mV. The differentiator prevents the tunnel diode discriminator from multiple pulsing if input signals are of long duration.

## 5. Output pulse generator and the fan-out Model CT

The circuit diagram is shown in Fig.5. This submodule consists of the monostable tunnel diode trigger D1, D2, the bistable tunnel diode trigger D3, the transistor switching circuit T3, T4, the output fan-out circuit T5-T12, and the VETO circuit T1. The monostable tunnel diode trigger generates pulses of 2 ns width. The bistable trigger is made monostable by the reset loop consisting of the T3, T4, T6, T11, coaxial cable and T2. The coaxial cable inserted in the reset loop determines the output pulse width. The fan-out delivers two nanosecond logic outputs N-LO and one inverse N-LO. The variation of the fan-out driving pulse amplitude (collector T4) was temperature compensated by means of the resistor-thermistor divider R22-R24.

## 6. Anticoincidence circuit

The circuit diagram (1) shown in Fig.6 represents the emitter coupled anticoincidence gate, intended for triggering the differential channel output. Input signals in differential discriminator (Fig.1D) are applied to both integral discriminators, which define the low- and high-levels of the differential channel. The output of the high-level discriminator is connected via delay lines ( $\ell =$ 10 cm and $\ell =$ 100 cm) to both veto-inputs of the anticoincidence gate. The output of the low-level discriminator is connected via delay line ( $\ell =$ 120 cm) to the anticoincidence gate input. In the case, where the input signal applied to the differential discriminator exceeds the low-level threshold and fails to exceed the high level threshold, positive output pulse is generated and transferred via the diode gate (2) in Fig.6 to the tunnel diode trigger (Fig.3, Fig.5). In the case, where the input signal also exceeds the high-level threshold, the veto-inputs prevent generating output pulse for the time interval of 10 ns. This is done to guarantee the anticoincidence to be performed within the limits defined by the time walking of high-level and low-level outputs, due to amplitude variation and finite risetime of the input pulses.

## 7. Diode attenuator-invertor and attenuator bifurcation

The circuit diagrams are shown in Fig.7. The diode attenuator-invertor employs the characteristics of p-i-n diode-twins[5]. It consists of the following functional parts: The input asymmetric-symmetric transformer, the controlled diode bridge, the output symmetric-asymmetric transformer and the control circuit for the continuous adjustment of the diode bridge attenuation (Fig.8C,D).

Specification

Input: Negative or positive P.M. pulse

Pulse amplitude: $<$ 100 V

Risetime: $\geq$ 1.4 ns

Dynamic range of input pulses: 100 mV - 100 V

Output: Negative or positive pulse

Risetime: $\leq$ 1.6 ns for an input risetime of 1.4 ns

Characteristic impedance: 100 ohms
Attenuation: 6 - 52 dB continuously
Reflections: < 26 dB
Feedthrough: <52 dB

The diode attenuator bifurcation is shown in Fig.7B. Input and output specification is the same as the specification of the diode attenuator-invertor.
Input characteristic impedance: 50 ohms
Output characteristic impedances: 100 ohms

When attenuation is varied in one of the two channels, the variation in the second one of the two channels is less than 2%.

*Module Specifications*

1. Quad Discriminator Model 5 NS
Block diagram: Fig.1A
Circuit diagrams: Figs.2,3,8AB
Module frontpanel: Fig.10A
Circuit board assembly: Figs.12,14
Printed circuit board: Fig.18
Operating mode: Four independent discriminators
Input: Negative photomultiplier pulse
Pulse amplitude: < 20 V
Input impedance: 100 ohms
Threshold: 50 mV for an input risetime of 2 ns
Threshold stability: 0.5% C
Input pulse pair resolution: 5 ns
Outputs: 2 N-LO, nanosecond logic outputs
1 N-LO, inverse nanosecond logic output
Pulse amplitude: 18 mA into 50 ohms matched coaxial cable
Risetime: 1.4 ns
Fall time : 2.2 ns
Pulse width: 5 ns FWHM
Output pulse pair resolution: 8 ns
Subnanosecond output SN-O: positive
Pulse amplitude: 7 mA into 50 ohms coaxial cable
Pulse width: 0.35 ns FWHM
Veto input: Nanosecond logic pulse
Pulse amplitude: $\geq$6 mA
Input impedance: 100 ohms
Operating temperature: 15-55 $^{o}$C.

2. Dual Discriminator Model 5NS
Block diagram: Fig.1A
Circuit diagrams: Figs.2,3,8AB
Module frontpanel: Fig.11A
Circuit board assembly: Figs.12,14
Printed circuit board: Fig.18
Operating mode: Two independent discriminators
Note: Specification is the same as the specification of the Quad Discriminator Model 5NS.

3. Quad Discriminator Model C=T
Block diagram: Fig.1B
Circuit diagrams: Figs.4,5,8AB
Module frontpanel: Fig.10B
Circuit board assembly: Fig.15
Printed circuit board: Fig.19
Operating mode: Four independent discriminators
Input: Negative photomultiplier pulse
Pulse amplitude: < 10 V
Input impedance: 100 ohms
Threshold: 50 mV for an input risetime of 2 ns
Threshold stability: 1% °C
Input pulse pair resolution: 10 ns
Outputs: 2N-LO, nanosecond logic outputs
1N-LO, inverse nanosecond logic output
Pulse amplitude: 18 mA into 50 ohms matched coaxial cable
Risetime: 1.8 ns
Fall time: 2 ns
Pulse width: 6 ns plus cable delay inserted
Veto input: Nanosecond logic pulse
Pulse amplitude: > 6 mA
Input impedance: 100 ohms
Operating temperature: 15-55 °C.

4. Dual Integral Discriminator Model 5 NS
Block diagram: Fig.1C
Circuit diagrams: Figs.7A,2,3,8ABCD
Module frontpanel: Fig.11A
Circuit board assembly: Figs.12,14
Printed circuit board: Fig.18
Operating mode: Two independent integral discriminators
Input: Negative or positive photomultiplier pulse
Pulse amplitude: <40V

Risetime: $\geq$ 1.4 ns
Input impedance: 100 ohms
Range of threshold adjustment: 100 mV-20V
Threshold stability: 0.5% °C
Input pulse pair resolution: 5 ns
Outputs: 2 N-LO, nanosecond logic outputs
1 N-LO, inverse nanosecond logic output
Pulse amplitude: 18 mA into 50 ohms matched coaxial cable
Risetime: 1.4 ns
Fall time: 2.2 ns
Pulse width: 5 ns FWHM
Output pulse pair resolution: 8 ns
Veto input: Nanosecond logic pulse
Pulse amplitude: $\geq$ 6 mA
Input impedance: 100 ohms
Operating temperature: 15-55 °C

5. Differential Discriminator Model 5NS
Block diagram: Fig.1D
Circuit diagrams: Figs.7B,2,3,6,8ABCD
Module frontpanel: Fig.11B
Circuit board assembly: Figs.14,16,13
Printed circuit board: Figs.18,20
Operating mode: Two independent integral discriminators with common input, controlling differential channel
Input: Negative or positive photomultiplier pulse
Pulse amplitude: < 40 V
Risetime: $\geq$1.4 ns
Input impedance: 50 ohms
Range of threshold adjustment:
Lower level: 100 mV - 20 V
Upper level: 200 mV - 40 V
Input pulse pair resolution: 10 ns
Integral and differential outputs:
2N-LO, nanosecond logic outputs
1N-LO, inverse nanosecond logic output
Risetime: 1.4 ns
Fall time: 2.2 ns
Pulse width: 5 ns FWHM
Output pulse pair resolution: 10 ns
Veto inputs: Nanosecond logic pulse

Pulse amplitude: $\geq$ 6 mA
Input impedance: 100 ohms
Operating temperature: 15-55 °C

6. Differential Discriminator Model 5 NS - CT
Block diagram: Fig.1D
Circuit diagrams: Figs.7B,2,3,5,6,8ABCD
View of the module: Figs.9,13
Circuit board assembly: Figs.14,17
Printed circuit board: Figs.18,21
Operating mode: Two independent integral discriminators with common input, controlling differential channel
Input: Negative or positive photomultiplier pulse
Pulse amplitude: < 40 V
Risetime: $\geq$ 1.4 ns
Input impedance: 50 ohms
Range of threshold adjustment:
Lower level: 100 mV - 20 V
Upper level: 200 mV - 40 V
Input pulse pair resolution: 10 ns
Integral outputs: 2 N-LO, nanosecond logic outputs
1 N-LO, inverse nanosecond logic output
Pulse amplitude: 18 mA into 50 ohms matched coaxial cable
Risetime: 1.4 ns
Falltime: 2.2 ns
Pulse width: 5 ns FWHM
Differential outputs: 2 N-LO, nanosecond logic outputs
1 N-LO, inverse nanosecond logic output
Pulse amplitude: 18 mA into 50 ohms matched coaxial cable
Risetime: 1.8 ns
Falltime: 2 ns
Pulse width: 6 ns plus cable delay inserted
Output pulse pair resolution: 10 ns
Veto inputs: Nanosecond logic pulse
Pulse amplitude: $\geq$ 6 mA
Input impedance: 100 ohms

## References


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3. P.Horvath, L.Ondris. IEEE Trans. Nucl.Sci., NS-18, No.1, 1971, 102.
4. P.Horvath. IEEE Trans. Nucl.Sci., NS-19, No.1, 1972, 534; Communication of the JINR, E13-6143, Dubna, 1971.
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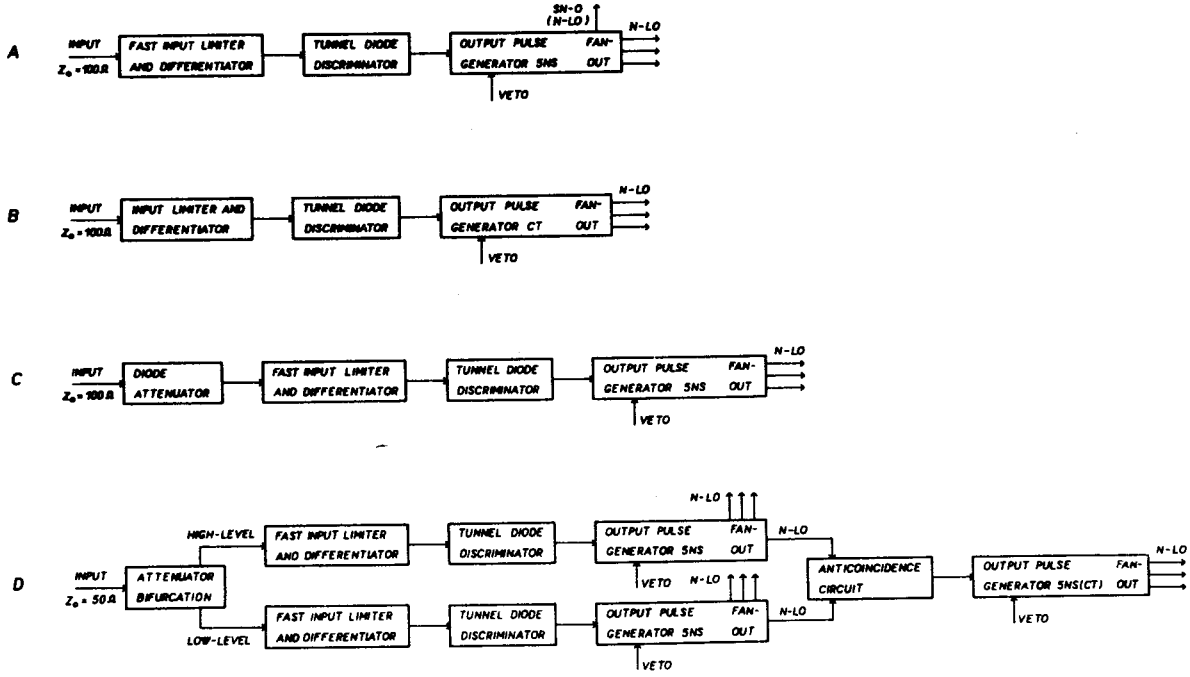



Fig.I. Block diagram of the fixed threshold discriminator Model 5NS (A), the fixed threshold discriminator Model CT (B), the integral discriminator Model 5NS (C), the differential discriminator Model 5 NS or Model 5 NS - CT (D).

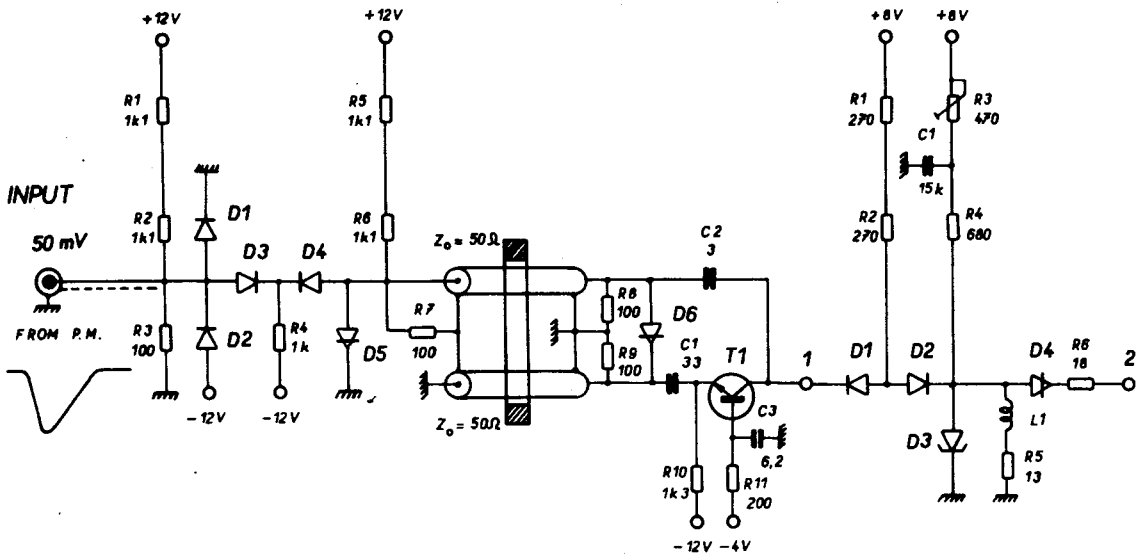



Fig.2. Submodules of the fast input limiter and differentiator Model 5NS (I) and the tunnel diode discriminator (2). Note (I): TI: GT330G; DI, D2: KD503B; D3,D4: ID508A; D5,D6: GI403A. Note (2): DI, D2: ID508A; D3: AI20IA; D4: AI402E.

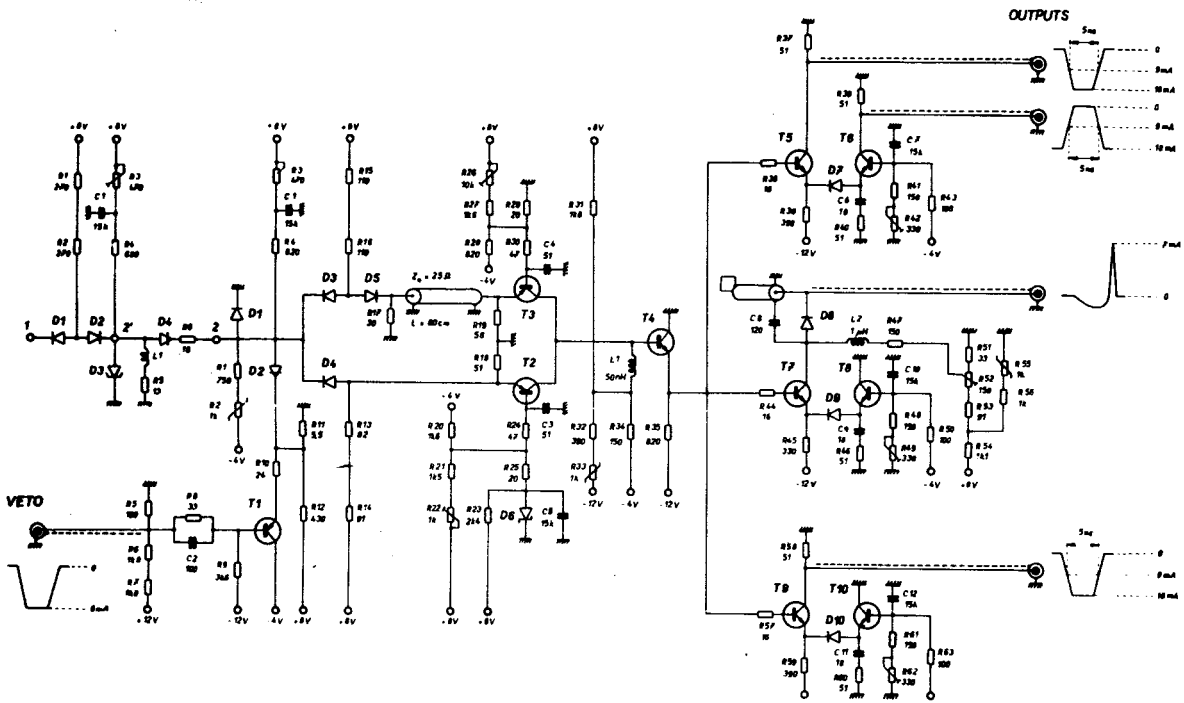



Fig.3. Submodules of the tunnel diode discriminator (I) and the output pulse generator and fan-out Model 5NS(2). Note (1): D1, D2: ID508A; D3: AI20IA; D4: AI402E. Note (2): T1-T3: IT3I3V; T4-T10: IT3III; D1: AI20IZH; D2: GI403A; D3-D5: KD5I3A; D6: 2SI07A; D7,D9,D10: KD503B; D8: D3I2.

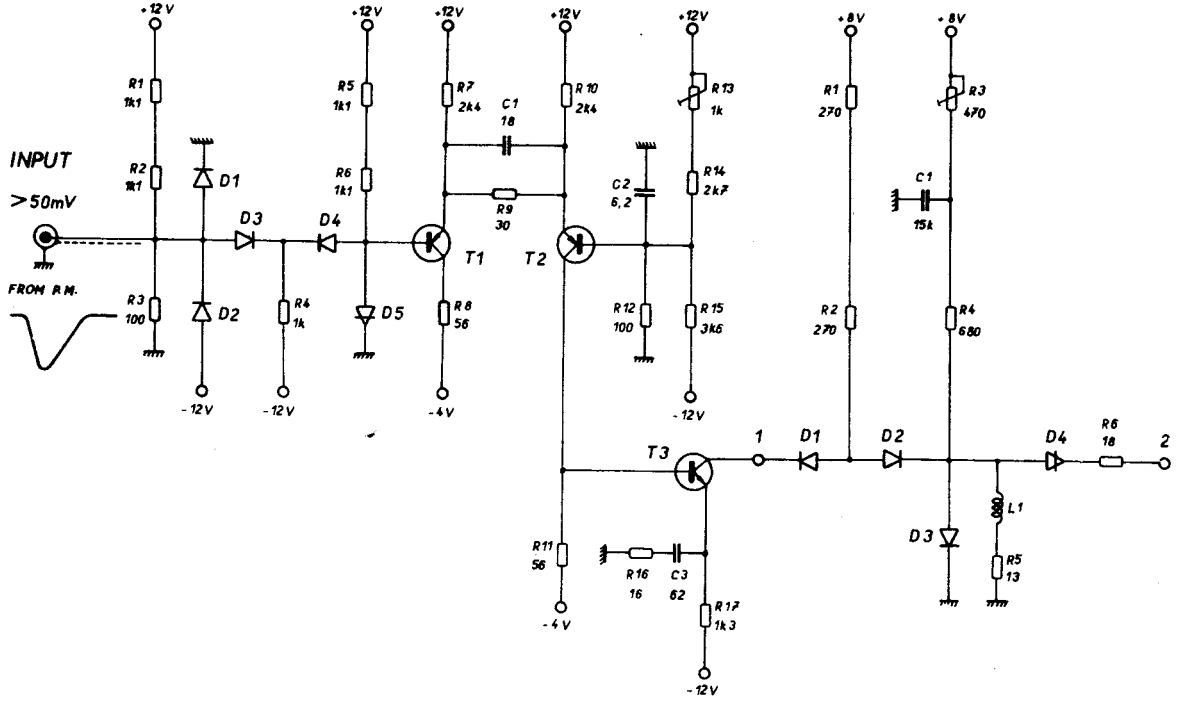



Fig.4. Submodules of the input limiter and differentiator Model CT (I) and the tunnel diode discriminator (2). Note (I): TI, T2, IT3I3V; T3: IT3III; DI,D2: KD503B; D3,D4: ID508A; D5: AI402E. Note (2): DI, D2: ID508A; D3: 3I306M; D4: AI402E.

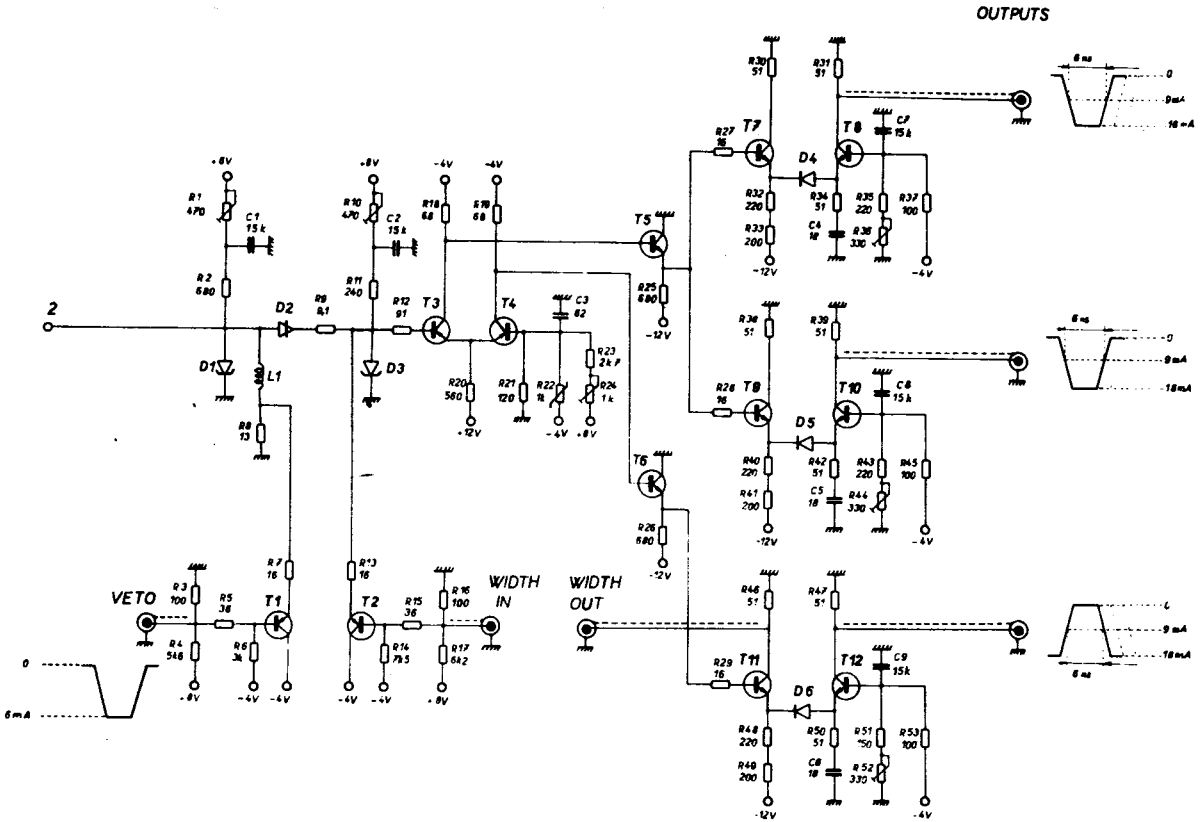



**Fig.5. Submodule of the output pulse generator Model CT. Note: T1-T4: IT313V; T5-T12: IT311; D1: 31306M; D2: AI402E; D3: AI201G; D4-D6: KD503B.**

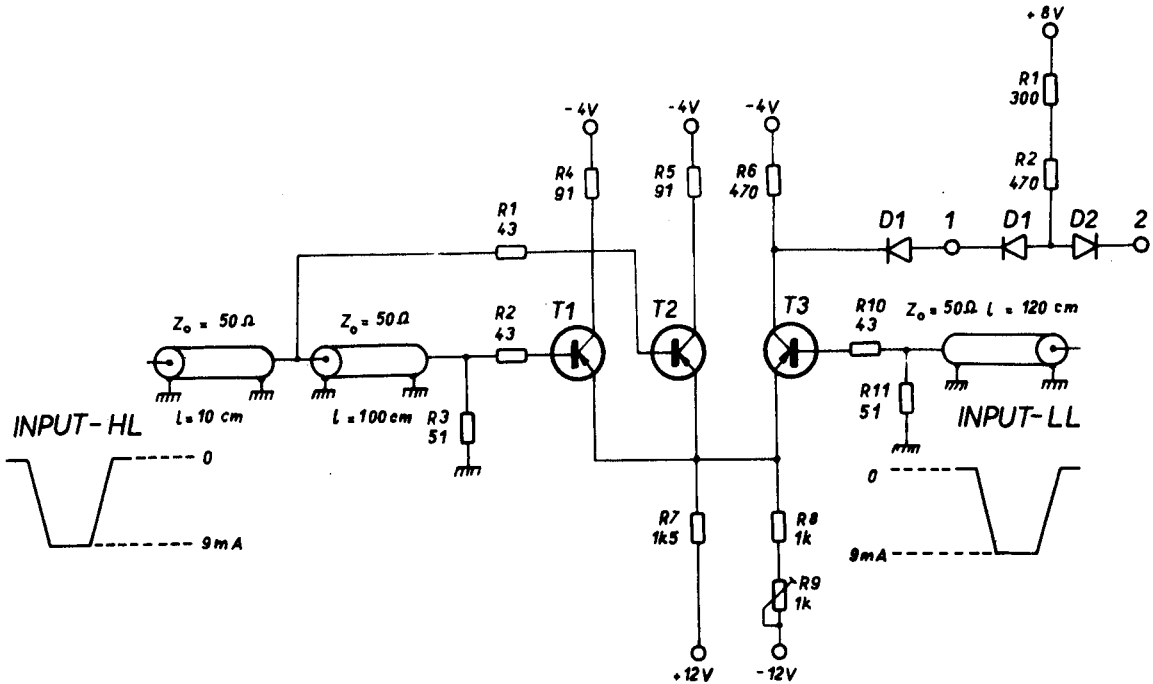



Fig.6.Submodule of the anticoincidence circuit (1) and the diode gate (2). Note (1): T1-T3: 1T313V; D1: ID508A. Note (2): D1, D2: ID508A.

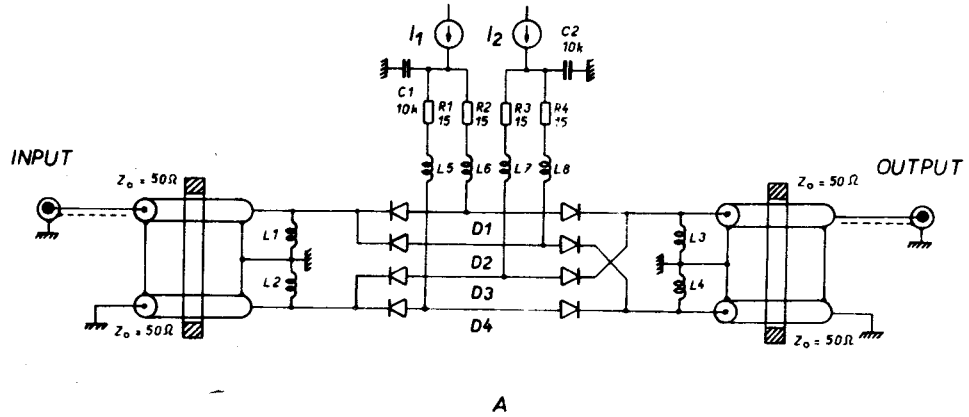
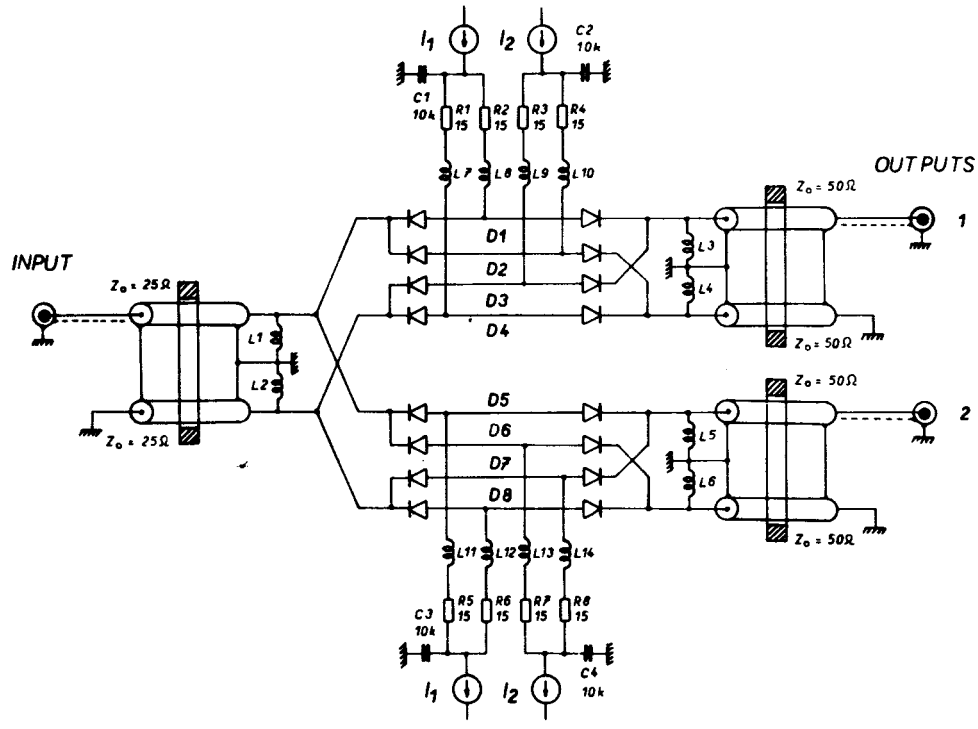
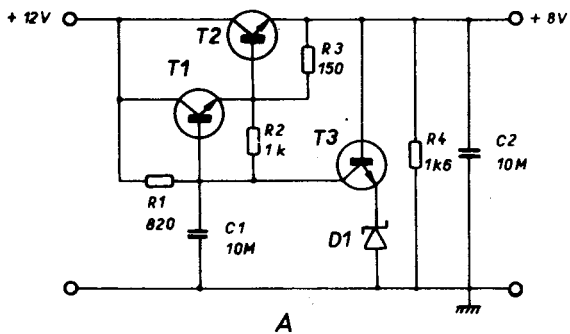
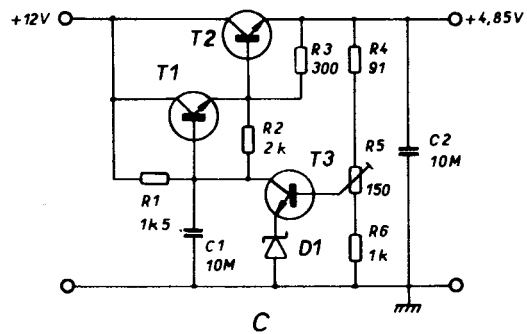


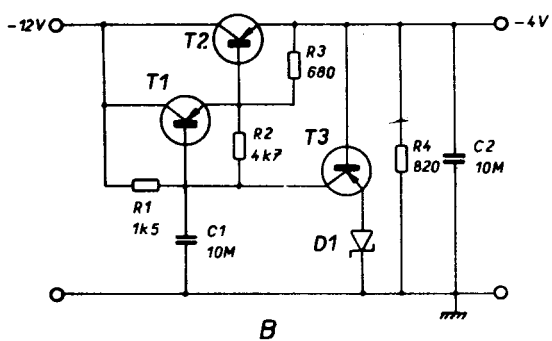

Fig.7. Submodules of the diode attenuator (A) and the attenuator-bifurcation (B).


INPUT
$Z_o$ = 25Ω
$Z_o$ = 25Ω
L1
L2
$I_1$
$I_2$
C2
10k
C1
10k
R1
15
R2
15
R3
15
R4
15
L7
L8
L9
L10
D1
D2
D3
D4
D5
D6
D7
D8
L11
L12
L13
L14
R5
15
R6
15
R7
15
R8
15
C3
10k
C4
10k
$I_1$
$I_2$
OUTPUTS
$Z_o$ = 50Ω
$Z_o$ = 50Ω
L3
L4
1
$Z_o$ = 50Ω
$Z_o$ = 50Ω
L5
L6
2

B



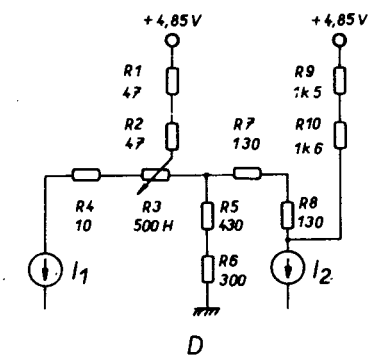




Fig.8. Submodules of the voltage stabilizers 8V, IA(A), -4V, 0.3A(B), 4.85V, 0.IA(C), the control circuit for the continuous adjustment of the diode bridge attenuation (D). Note (A): TI: KT602A; T2: P702; T3: KT3I5; DI: D8I4A. Note (B): TI, T3: MP4IA; T2: P304; DI: KSI39A. Note (C): TI, T3: KT3I5; T2: P70IA; DI: KSI39A.

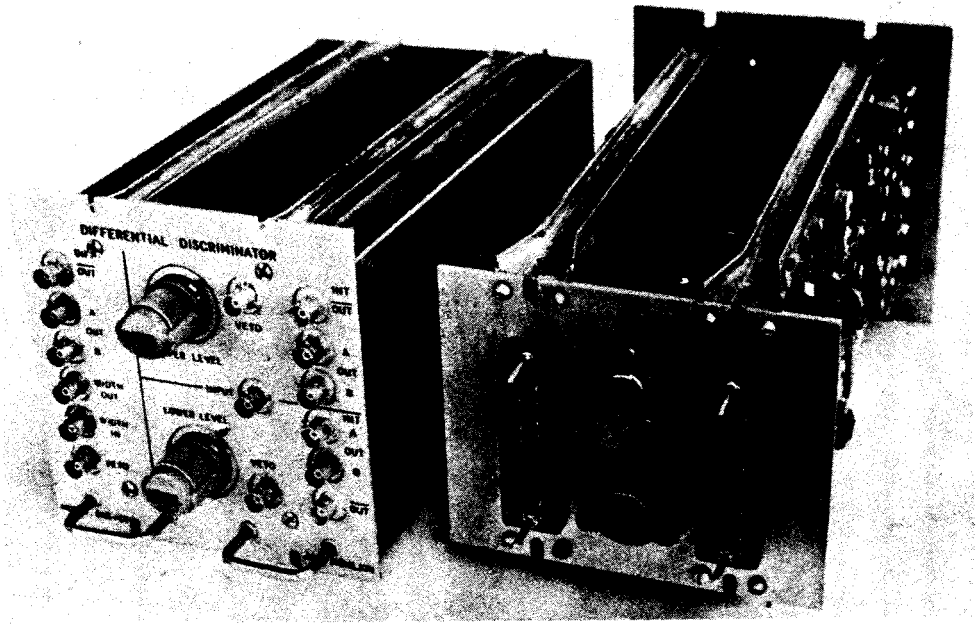



Fig.9. View of the module: Differential Discriminator Model 5 NS-CT.


(A)

Fig.10. View of the module frontpanels: Quad Discriminator Model 5 NS (A), Quad Discriminator Model CT (B).


(B)


DUAL
DISCRIMINATOR
DUAL
DISCRIMINATOR
INTEGRAL
THRESH
IN
VETO
OUT
A
B

(A)


(B)

Fig.II. View of the module frontpanels: Dual Discriminator Model 5 NS and Dual Integral Discriminator Model 5 NS (A), Differential Discriminator Model 5 NS (B).

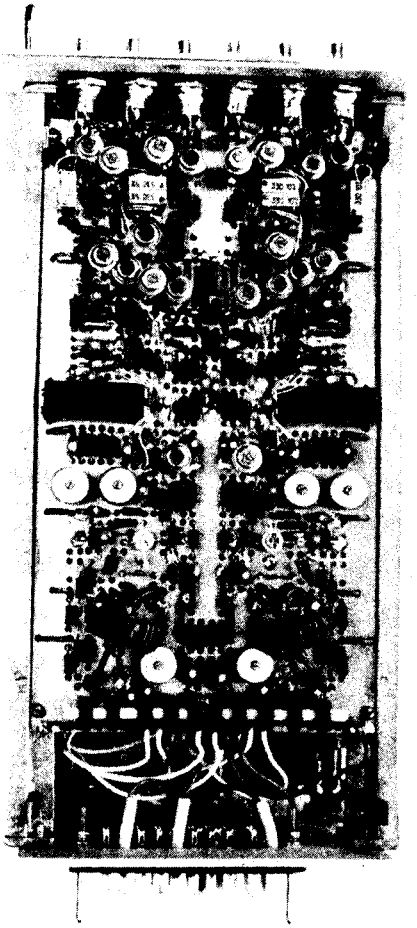


Fig.12. Quad Discriminator Model 5 NS, right side of the module, shield removed.

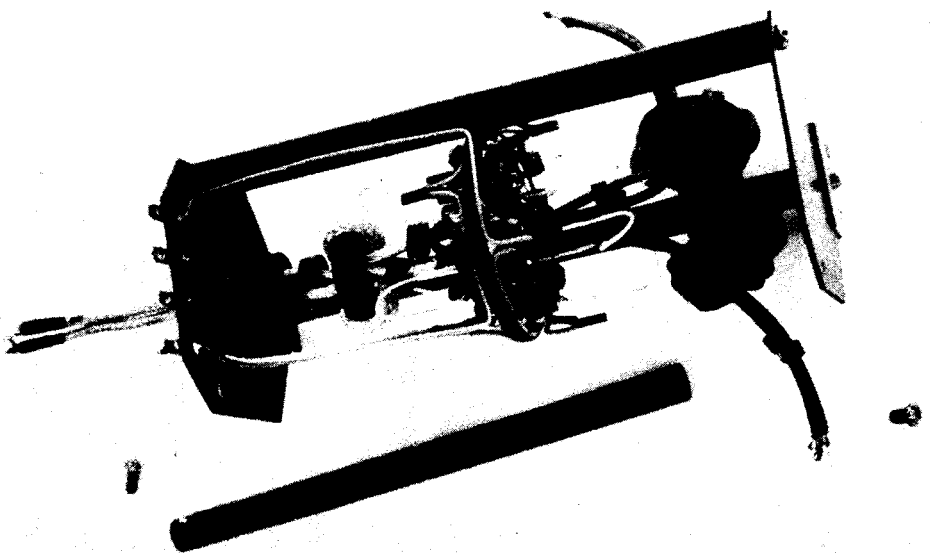


Fig.13. View of the submodule: Attenuator bifurcation.

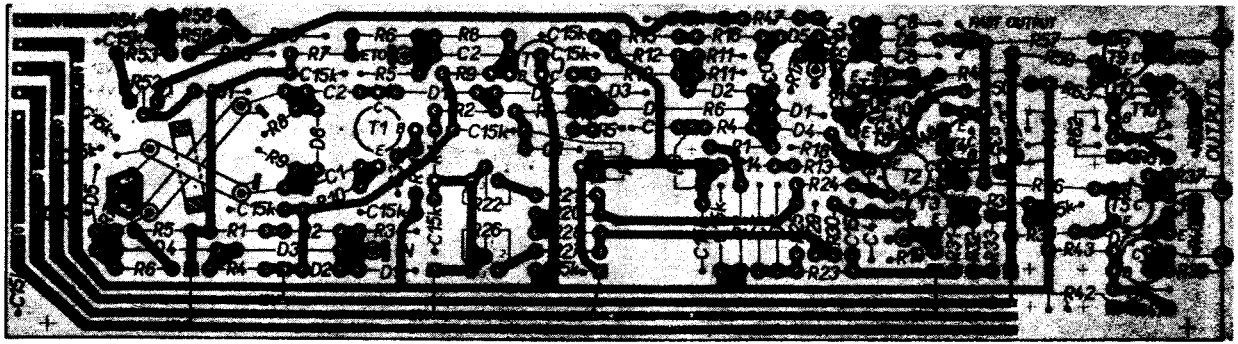


Fig.14. Fixed threshold discriminator Model 5 NS circuit board assembly, bottom part of the circuit board.

Fig.15. Fixed threshold discriminator Model CT circuit board assembly, bottom part of the circuit board.

Fig.16. Anticoincidence circuit and Output pulse generator Model 5NS circuit board assembly, bottom part of the circuit board.



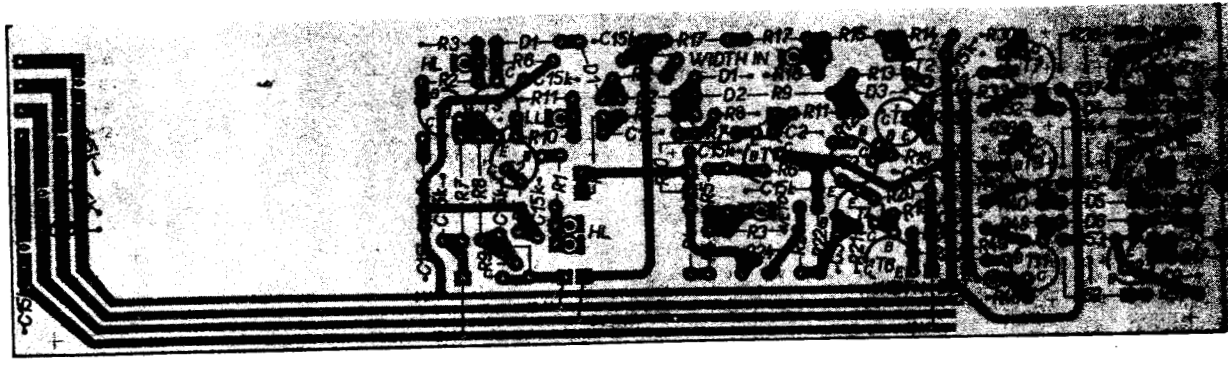



Fig.17. Anticoincidence circuit and Output pulse generator Model CT circuit board assembly, bottom part of the circuit board.

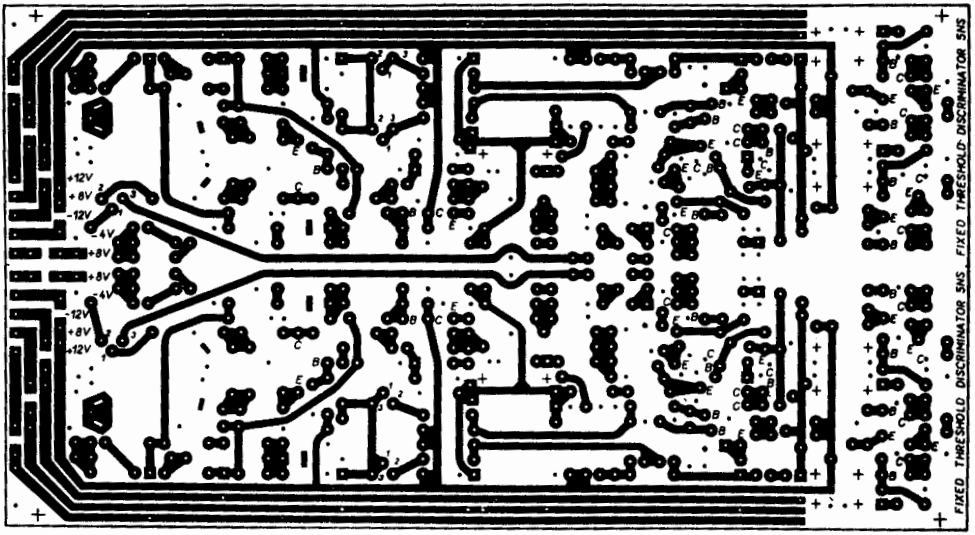



Fig.I8. Dual Fixed threshold discriminator Model 5 NS, printed circuit board.

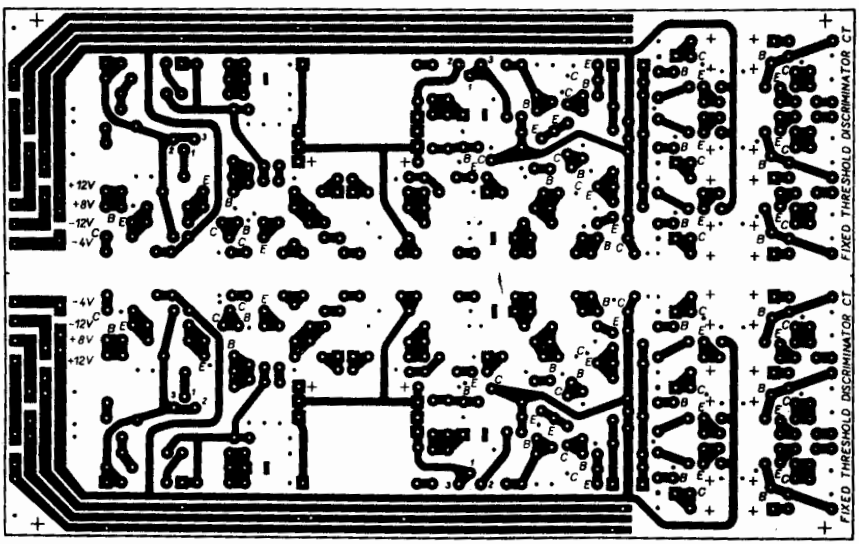



Fig.I9. Dual Fixed threshold discriminator Model CT, printed circuit board.

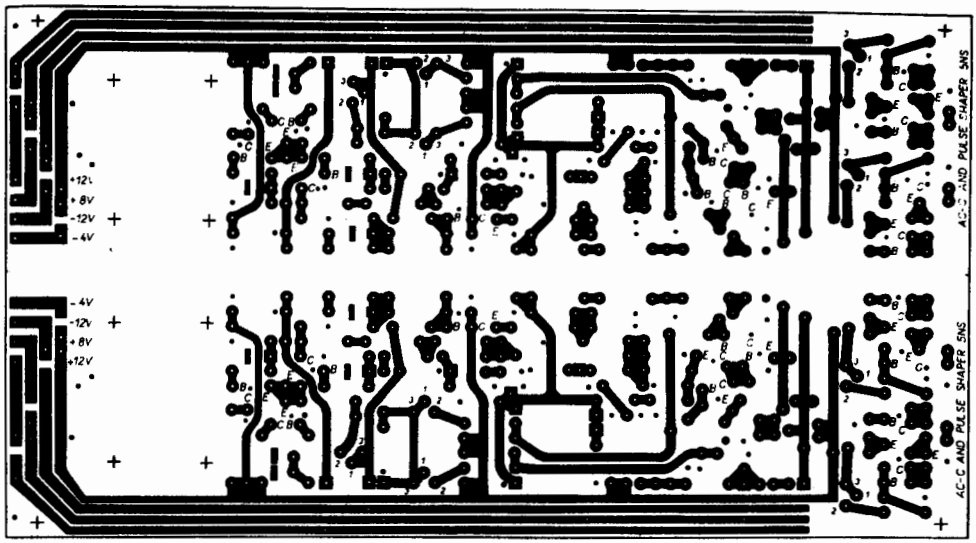



Fig.20. Dual Anticoincidence circuit and Output pulse generator Model 5 NS, printed circuit board.

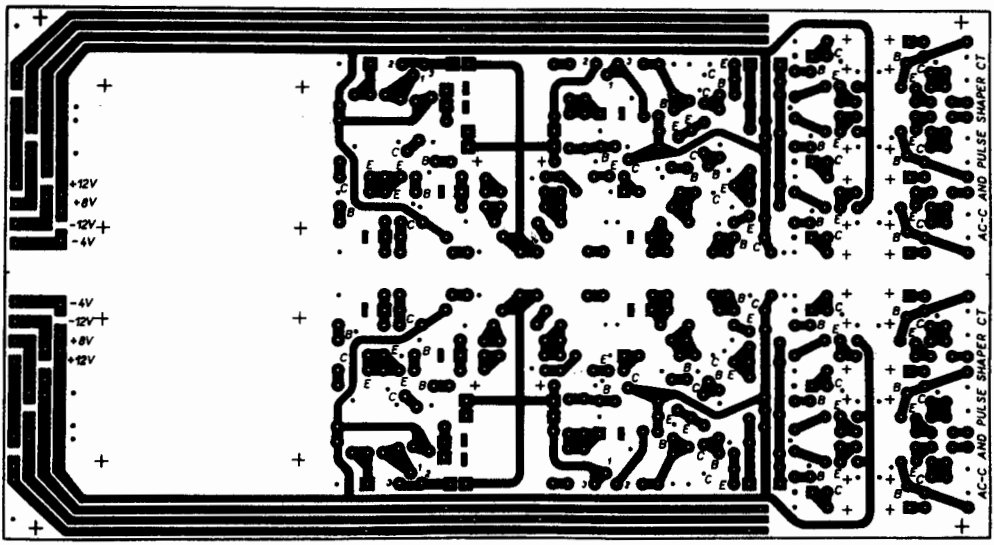



Fig.21. Dual Anticoincidence circuit and Output pulse generator Model CT, printed circuit board.