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FAST ELECTRONIC MODULES FOR A SUBNANOSECOND COINCIDENCE -ANTICOINCIDENCE LOGIC

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* On leave from Czechoslovak Academy of Sciences, Praha, CSSR.

Introduction

This paper is the continuation of the work[1] and contains some results of the experience with the Fast electronic modules previously reported. This work gives information about representative circuits and about the construction of modules, intended to build subnanosecond coincidence-anticoincidence logic and a supervisory nanosecond logic in high energy physics experiments. These modules are to work reliably in laboratory conditions, over the large room temperature range, with very high counting rates and with the wide dynamic range of input pulses. The modules are made up of a number of simple basic circuits, submodules. The function of each submodule is indicated in Fig. 1. Each submodule could be operated independently and thus the versatility of the system was achieved. In the following sections modules and submodules are shortly described and technical parameters are presented. The more complete description and documentation would be available in preprints of the JINR, Dubna, which are prepared for publication.

Module Description

1. Modules containing fixed threshold and continuously variable threshold discriminators

These modules have been designed for front-edge timing and for amplitude selection of photomultiplier pulses. The block diagram of the continuously variable threshold discriminator is shown in Fig. 1A. The fixed threshold discriminator has the same structure, except the input attenuator-invertor, full circuit diagram is shown in Fig. 2. Inside the one module with front panel of dimension 80 x 160 mm^2 are inserted two complete discriminators. In every discriminator the INPUT, the VETO and three of the nanosecond logic outputs N-LO are laid out to the front panel connectors. BNC connectors are used. One of N-LO or the SN-0 subnanosecond output is used inside the module, for instance for coincidence or anticoincidence operation (see below). With reference to the block diagram of Fig. 1A and circuit diagram of Fig. 2, the functional submodules are the following:

Input Limiter

In this functional submodule the circuit consisting of the diodes D1-D6, and the asymmetric-symmetric transformer is used. This circuit has been derived from a symmetric limiter, described in [2]. In contrast to circuits described previously [1,3] no transistors are used in this limiter and thus the better efficiency of limitation, a wider dynamic range of input pulse amplitudes and higher rate of operation was achieved.

Differentiating circuit

The differentiation is obtained by the differentiating RC circuit, consisting of the capacitor C1 and of the input impedance of the common base transistor T1. The resistor R7 and the capacitor C2 are balancing elements, balancing the output of the differentiating circuit, with respect to the asymmetric connection of the differentiating circuit to the limiter.

Tunnel diode descriminator

The tunnel diode discriminator consists of the diodes D7-D9. The tunnel diode D9 is operated in the monostable mode, generating pulse of 2 ns width.

Output pulse generator and the fan-out

The output pulse generator, the fan-out and the veto circuit are functionally identical with the ones described in[1] and differ mainly by the application of temperature compensation circuits. The monostable tunnel diode trigger D11, D12 generates pulses of 1 ns width, the output pulse generator has the maximum rate of operation above 200 MHz . The fan-out delivers dual nanosecond logic outputs N-LO and the subnanosecond output SN-0. Two of N-LO are negative output pulses, one of N-LO is a dual positive output pulse.

The output pulse generator and the fan-out contain the temperature compensation circuits. The drift of tunnel diode D11 bias current, which is also dependent on the associated elements D13 - D15, T3, T4 was temperature compensated by means of the resistor-thermistor divider R18, R19. The drift of the pulse amplitude of nanosecond logic output pulses was temperature compensated by means of the resistor-thermistor divider R48 - R50. The drift of the timing pulse of the subnanosecond output was temperature compensated by means of the resistor-thermistor divider R68 - R73. Temperature compensation of the tunnel diode bias current drift and timing pulse drift must be adjusted individually in every discriminator. The application of a circuit for temperature compensation of the tunnel diode D9 bias current drift does not seem necessary in our fixed threshold discriminator. The reliable performance of modules could be achieved also without temperature compensation circuits. However, temperature compensation extends reliable performance of modules over the temperature range of 15 - 55^{o}C.

Specification

Fixed threshold discriminator

Input: Negative photomultiplier pulse

Pulse amplitude: < 20V

Input impedance: 100 Ω

Threshold: 50 mV for an input risetime of 2ns.

Threshold stability: 0.5 %/^{o}C

Signal resolution: 5 ns

Outputs: 2 N-LO, negative

1 N-LO, dual, positive

Pulse amplitude: 18 mA into 50 Ω

matched coaxial cable

Risetime: 1.4 ns

Falltime: 2.2 ns

Pulse width: 5 ns FWHM

1 SN-O, positive

Pulse amplitude: 7 mA into 50 Ω

coaxial cable

Pulse width: 0.35 ns FWHM

Operating temperature: 15 - 55^{o}C.

2. Diode attenuator-invertor

The diode attenuator-invertor (Fig. 3), employs the characteristics of microwave switching diode twins. It consists of the following functional parts: the asymmetric-symmetric transformer, the controlled diode bridge, the output symmetric-asymmetric transformer and the control diode bias current circuit. The attenuation of the diode bridge is controlled by the bias currents I_1, I_2. The corresponding values of the bias currents I_1,I_2 (mA) and attenuation (dB) for the characteristic impedance of the diode bridge Z_0 = 100 Ω are shown in the diagram (Fig. 4).

Specification

Diode attenuator-invertor

Input: Negative or positive pulse

Pulse amplitude: < 100 V

Risetime: > 1.4 ns

Flat top: ≤ 20 ns

Output: Negative or positive pulse

Risetime: < 1.6 ns for an input risetime of 1.4 ns

Attenuation: 6 - 46 dB continuously

Reflections: < 26 dB for an input resetime of 1.4 ns

Feedthrough: < 52 dB for an input risetime of 1.4 ns

Note: The attenuation over the range of 0.9 - 46 dB can be achieved for the corresponding values of diode bias currents of approximately 200 mA. From this practical point of view, the attenuator was designed for the attenuation of 6 - 46 dB.

3. Differential and integral discriminator

The differential and integral discriminator (Fig. 1B) was composed from submodules, describe in the previous sections. The performance required of this module was to achieve the high counting rates and the signal resolution of the same order, as has been achieved with timing modules. No extreme requirements on threshold and channel width stability were required. An input signal is applied to the two fixed threshold discriminators, via an asymmetric to symmetric transformer, diode attenuators and symmetric to

asymmetric transformers. By means of diode attenuators, low and high discriminating levels are adjusted. The differential channel output pulse generator is triggered from the anticoincidence circuit AC-C. The output pulse generator and the fan-out are of the cable timed type, with the adjustable output pulse width.

Specification

Differential and integral discriminator

Input: Negative or positive photomultiplier pulse

Pulse amplitude: < 40V

Risetime: ≥ 1.4 ns

Input impedance: 50 Ω

Operating mode: Two independent integral discriminators, controlling common differential channel.

Integral discriminator:

Dynamic range of threshold: 100 mV - 20 V

Signal resolution: 5 ns

Threshold stability: 0.5 %/^{o}C

Outputs: 2 N-LO negative

1 N-LO dual, positive

Pulse amplitude: 18 mA into 50Ω matched coaxial cable

Risetime: 1.4 ns

Falltime: 2.2 ns

Pulse width: 5 ns FWHM

Differential channel:

Outputs: 2 N-LO negative

1 N-LO dual, positive

Pulse amplitude: 18 mA into 50Ω matched coaxial cable

Risetime: 2 ns

Falltime: 3 ns

Pulse width: ≥ 5 ns FWHM cable timed

Operating temperature: 15 - 55°C.

4. Many-fold coincidence system

The module, many-fold coincidence system (Fig. 1C) contains four fixed threshold discriminators. The subnanosecond outputs are laid into the fast coincidence circuit (Fig. 5), which presents the fast-slow coincidence system composed of 6 two-fold coincidence units with a time resolution of 0.5 ns FWHM and of six-fold coincidence unit with a time resolution of 10 ns. The tunnel diode discriminator, the output pulse generator and the fan-out are identical with submodules described in previous sections. The module contains the switch selector which controls the operating mode of the many-fold coincidence system.

Specification

many-fold coincidence system

Inputs: Negative photomultiplier pulses

Pulse amplitude: < 20 V

Input impedance: 100 Ω

Operating mode: 1. Two-fold coincidence operation 2CC12-2CC34
2. Majority two-fold coincidence operation 2CC1234
3. Three-fold coincidence operation 3CC123-3CC234
4. Majority three-fold coincidence operation 3CC1234
5. Four-fould coincidence operation 4CC1234

Time resolution: 0.5 ns FWHM for all operating modes

Stability of the time resolution with time: ± 10 ps/ 24 hours.

Note: Specifications of the fixed threshold discriminators and coincidence channel submodules are identical with the ones reported in section 1.

Conclusions

A system of fast electronic modules for the subnanosecond timing and logic operation has been designed to meet many of physicists' requirements in high energy physics experiments. The signal resolution, the wide dynamic range of input pulses , the time resolution and good temperature stability should enable the modules to perform many operations also in some other nuclear physics experiments.

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References

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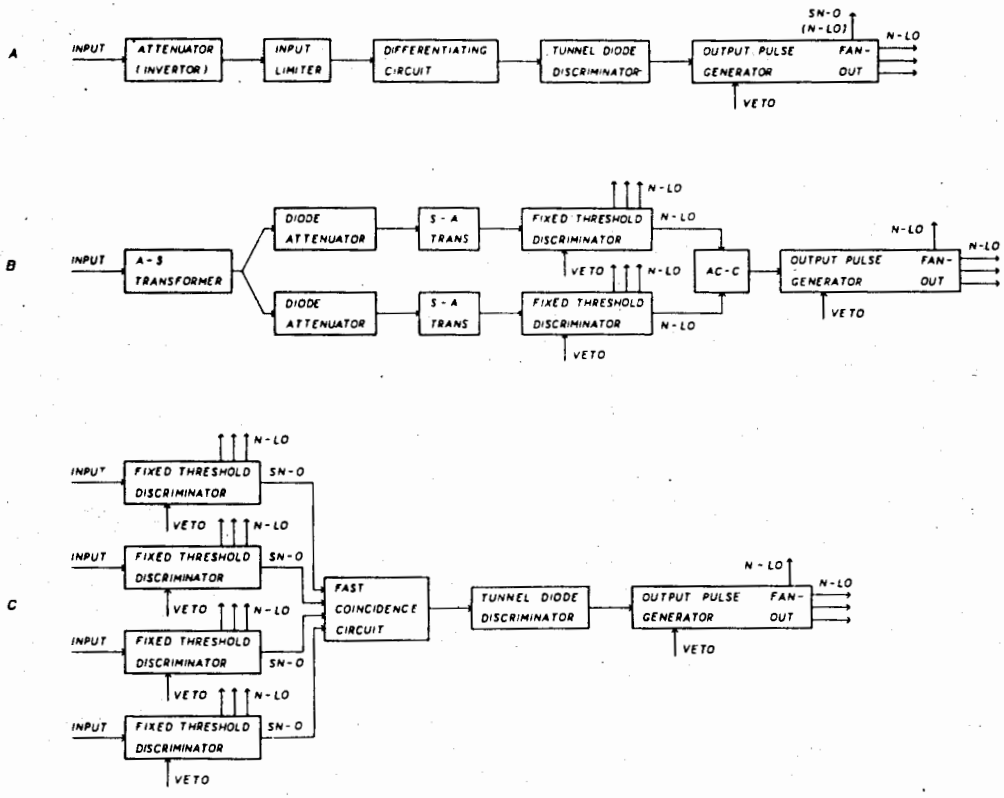

Fig. 1. Block diagram of the continuously variable threshold discriminator (A), the differential and integral discriminator (B), the many-fold coincidence system (C).

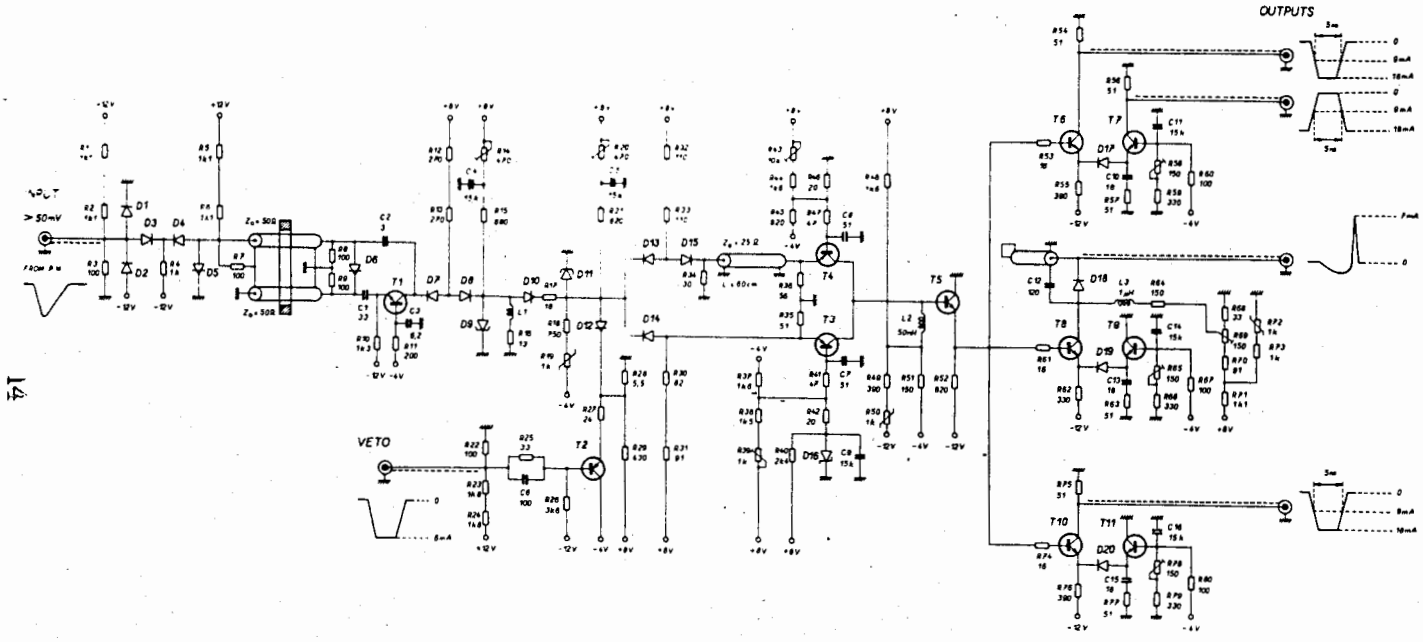

Fig. 2. Fixed threshold discriminator. Note: T1: f_T = 1GHz; T2-T4: 1T313V; T5-T11: 1T311I; D1, D2, D17, D19,D20: KD503B; D3, D4, D7, D8: 1D508A; D5, D6, D12: GI403A; D9: AI201A; D10: AI402E; D11: AI201ZH: D13, D14, D15: KD513A; D16: 2S107A; D18: D 312.

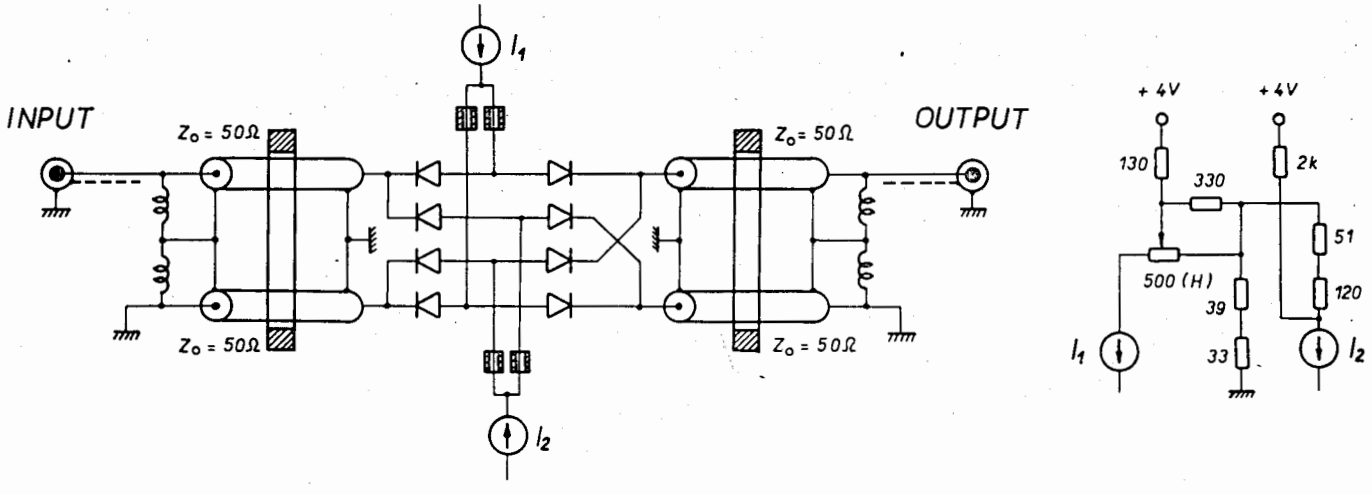

Fig. 3. Diode attenuator-invertor

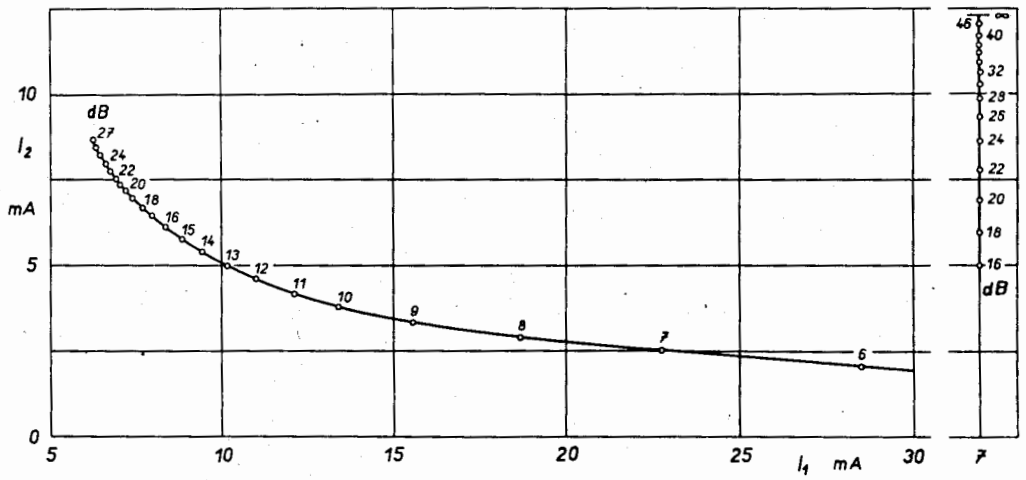

Fig. 4. Corresponding values of the bias currents and attenuation.

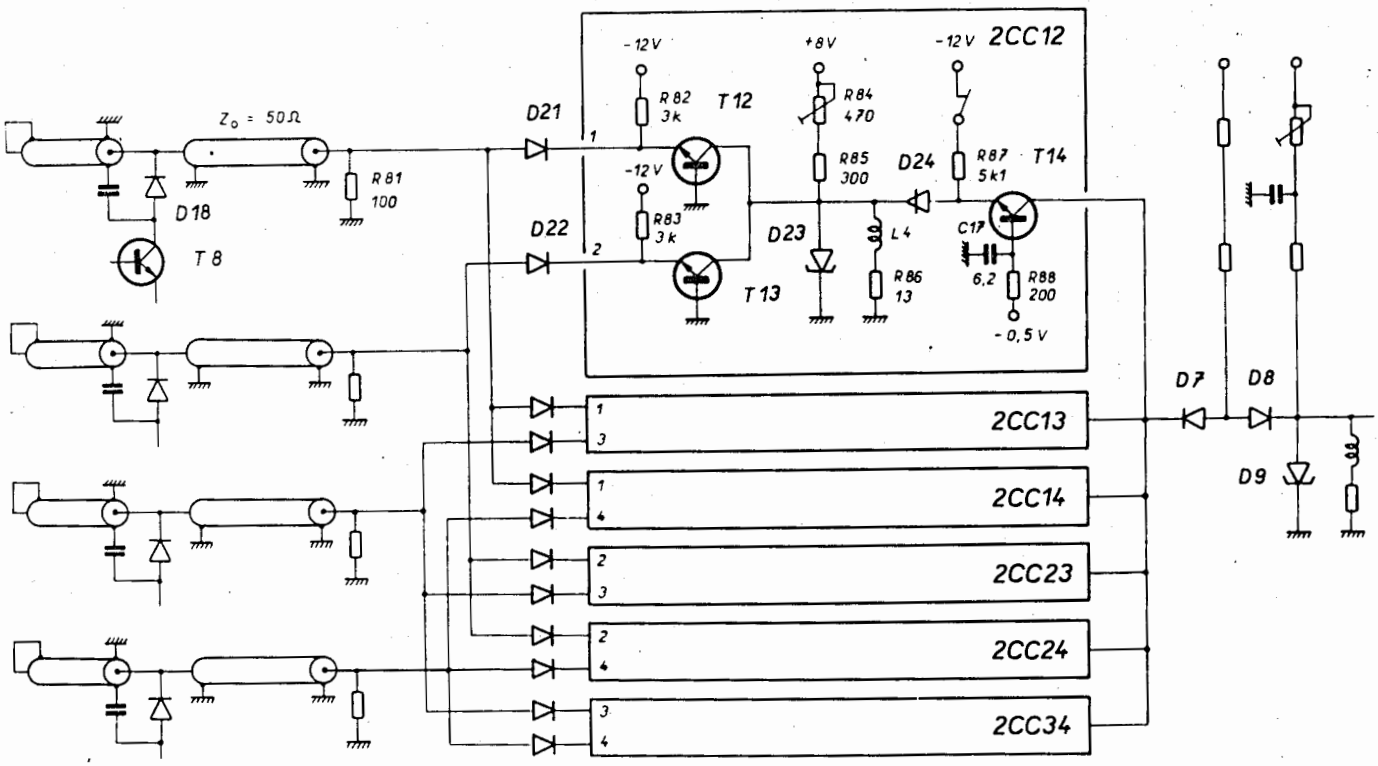

Fig. 5. Fast coincidence circuit. Note: T12, T 13: f_T= 1.5 GHz; T14: f_T = 1 GHz; D21, D22: 1D508A; D23: 3I306M; D24: AI402E.