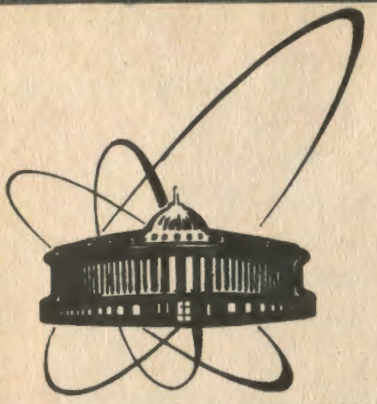

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VIDEOMEMORY MODULE FS-4 FOR PERSONAL COMPUTERS IBM PC XT (AT)

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VIDEOMEMORY MODULE FS 4

INTRODUCTION

Module FS 4 (Frame Storage 4) for IBM PC XT (AT) personal computers is discussed. The module is a part of the processing system of the image obtained by the CCD - camera (Fig.1). Internal frame buffer can store up to four 256-by-256 pixels images with 8-bit resolution (256 levels of grey). The digitized image is written into a selected memory plane via the fast serial channel at a transfer rate up to 15 MB/s. Any of the four memory planes can be mapped into PC operating memory space as one 64K block. The module has also a service (cursor) layer 256-by-256 pixels with 1-bit resolution. The contents of both this layers and the selected frame buffer plane can be monochromatically displayed by 9-bit video DAC.

The whole plug-in module is placed on two printed circuit boards. The boards are connected together and occupy on PC-bus two slots of a full length. On the back side of one of the boards there are a 25-pin connector for coupling to the image digitizer block and a BNC connector as a video output. The module takes up in the PC-I/O space four adjacent ports.

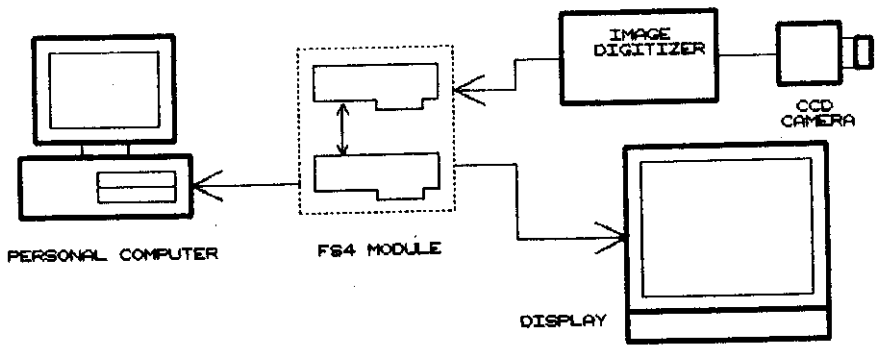

Fig.1. Image processing system.

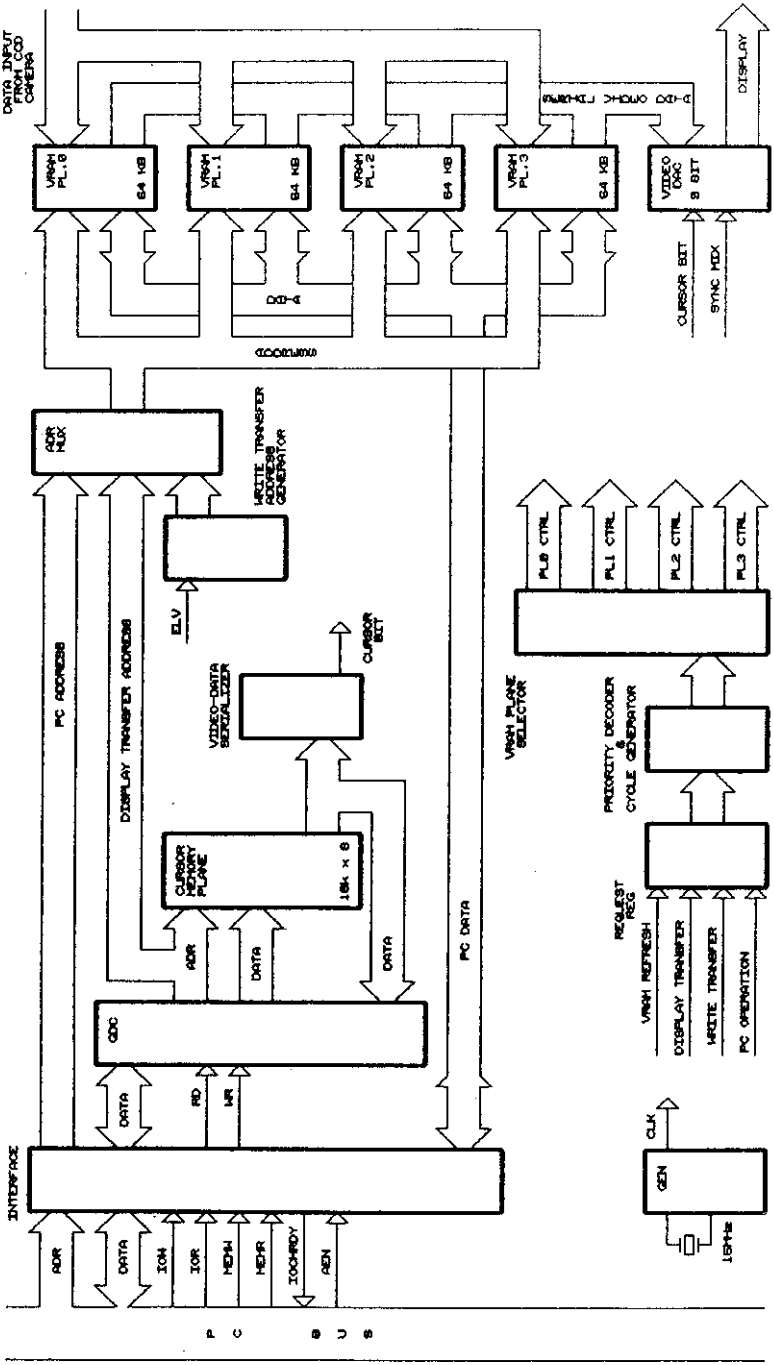

FIG.2. FRAME STORAGE 4 BLOCK SCHEME

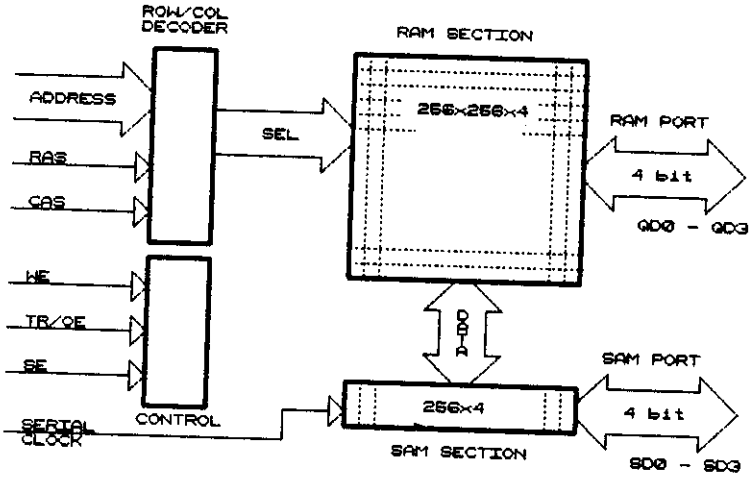

Fig.3. Block scheme of MB82461.

Their base address can be changed by using a jumper. The address of the 64K block of PC operating memory assigned to one of the videomemory planes can be changed in the same manner. All the rest of control functions is executed by software.

I. DESCRIPTION OF THE INVESTIGATION

The block scheme of the FS 4 is depicted on Fig.2.

a) Frame buffer

The basic part of FS 4 is four memory planes. Each of them is based on two MB81461 IC's of the firm Fujitsu which represent memory of "Video RAM" (VRAM) type [1]. The chip of memory consists of two independent sections (Fig.3).

The RAM-section (64k x 4) holds image and is accessible for PC as a part of operating memory. The RAM-section of MB81461 is organized as 256x256x4 block. The RAM-section has all operating modes, occuring in memory of DRAM type (read mode, write mode, read-modify-write mode, page mode).

For fast bidirectional data transfer memory contains SAM-section (Serial Access Memory). The SAM represents a shift register of 256x4 bit. The contents of the register can be pushed or pulled with a frequency up to 20 MHz. Serial access is completely independent of the RAM-section operation. The interaction of the RAM and SAM sections takes place in the transfer cycle only. The transfer cycle allows one to copy in one specific memory cycle the contents of any row of the RAM-section into the SAM-section and vice versa. This permits one to display data and simultaneously to execute a memory read or memory write operation between PC and the RAM-section of VRAM.

b) Operations with VRAM memory

As it is clear from the description of the integrated circuit MB81461, four different operations with VRAM memory should be provided:

- Write Transfer - a transfer of the SAM contents to the selected row of the RAM-section. This cycle is used while transferring data from the digitizer block into VRAM.
- Display Transfer - a transfer of the contents of the selected row of the RAM-section into SAM. It is used when preparing the output of a TV-line onto the display.
- Memory Operation - memory read and memory write operation between the computer and the RAM-section.
- Refresh Operation - one cycle of this operation refreshes one RAM-section row selected by the internal counter.

All the operations come about in synchronism with a clock signal (1.875 MHz). Every cycle is specified by the *cycle generator*. FPLA of 556PT1 (82S101) forms its basis. The request for one of the four operations is asynchronically latched into a *request register*. The *priority decoder* resolves conflict conditions, the highest priority is being given to the executed operation. Next in order of priority is the

Write-Transfer operation. The request for this operation generates a signal ELV (External Line Valid) that comes from the camera and indicates SAM filled with one line. The third in priority is the memory operation command. It occurs at the access of PC to the RAM-section of VRAM. FS 4 requires a wait state in PC. As soon as the priority decoder determines the corresponding cycle is initiated and all necessary signals are generated; then the wait state and the whole cycle ends. The fourth priority belongs to the Display-Transfer command that is called up before the active line begins so that a possible delay couldn't affect the quality of the image. The lowest priority is given to the refresh cycle and therefore it is called up more often than it is required.

Some cycle make use of different addresses. Memory operation uses an address generated directly by PC. For Write-Transfer an address from the line counter is used. This counter is incremented by ELV signal. Data-Transfer employs the address generated by the GDC circuit described below. Refresh operation does not need an external address. The corresponding sources of addresses are switched by the *adrmux* block.

The *cycle generator* produces all necessary signals: RAS, CAS, ROW, TROE, WE and others. Signals are distributed by *vram plane sel* block based on PROM 74S287.

c) Graphics Display Control

The Graphics Display Controller - NEC μPD 7220A [2,3,4] is used to perform a generation of synchrosignals for display (VSYNC, HSYNC) and as a source of the address for Display Transfer. Its basic function is to operate a one-bit service layer. The layer is realized by two integrated circuits SRAM 8Kx1 - HM6264. Storage capacity of this memory allows producing of two switchable service layers for a size of 256x256 pixels. The flexible GDC control permits the service layer to be configured in another way: for instance, as a plane 384x256 pixels for the image menu at the edge of the screen.

d) Interface

The communication between FS4 and PC is provided by the interface that separates PC-bus from FS4 module, offers selection of ports and memory blocks and includes input and output status register.

II. FS 4 MODULE CONTROL

a) PC - FS 4 Communication

For an user the control of FS 4 module represents a communication with three input and three output ports:

STATUS GDC READ - reading of GDC status.

FIFO GDC READ - reading of GDC data (the cursor layer).

OUTPUT STATUS BUFFER READ - reading of the current state of data transfer from the camera into FS 4 module.

GDC COMMAND WRITE - writing of commands into GDC.

GDC PARAMETER WRITE - writing of parameters into GDC.

INPUT STATUS REGISTER WRITE - writing of the FS 4 control word.

GDC is controlled by a sequence of commands and parameters allowing one to determine completely the size of the cursor layer, to change its contents and to determine time parameters of composite video signal. GDC programming has been considered in detail in [4].

The cooperation with VRAM is controlled by writing of the control byte into the INPUT STATUS REGISTER:

	WP1	WP0	DP1	DP0	MP1	MP0	-	-
bit	7	6	5	4	3	2	1	0

- Memory Page 0, 1 (MP0, MP1) : two bits indicating which of the four VRAM planes will be mapped into the PC operating memory space.
- Display Page 0, 1 (DP0, DP1) : two bits indicating which of

the four VRAM planes will be displayed.

- Write Page 0, 1 (WP0, WP1) : two bits indicating in which of the four VRAM planes the digitized image will from the camera be written.

OUTPUT STATUS BUFFER allows the user program to check whether the write from the camera into FS 4 is finished or not. Only bit 0 of OSB is valid.

b) CCD - FS 4 Communication

The image transfer is initialized by the image digitizer block. The block is connected to FS 4 module by 25-pin CANNON connector. Apart from 8-bit data, into the module come additional three signals : External Frame Valid (EFV), External Line Valid (ELV) and External Data Valid (EDV). EFV signal becomes active before the data transfer is initiated and it is canceled after the frame transfer is finished. ELV signal becomes active before the sending data of each line and ends after the transfer of the whole line (256 pixels). Between lines it is in an inactive state. EDV signal represents a data strobe.

Data-Transfer from the digitizer refers to that plane of VRAM which has been already selected in ISR. The active state of EFV signal begins the data transfer.. Its initiation calls up Write Transfer request. This first cycle called up by this request will write into VRAM dummy data. Its task is to give a message to VRAM plane that the following shift pulses coming into the SAM will push new data from the digitizer into SAM (as apposed to a normal state, when the shift pulses with a frequency 7.5 MHz pull data from SAM to display the image). Then the ELV signal becomes active , and it enables the input of data. Data from the digitizer block come onto the inputs of SAM. Their validity proves EDV signal that simultaneously acts as shift clock and pushes gradually data into SAM. After the transfer of each line ELV signal becomes

inactive and its falling edge calls up the Write-Transfer cycle that copies the SAM contents into RAM. The number of the RAM-section row into which rewrite will be taken, is determined by ELV pulses counter. This way is used to transfer all 256 rows of a frame. The end of EFV signal can be tested by reading OSB.

III. CONCLUSION

FS 4 module has been used in PC-XT for the digitized image from "One - Shot CCD camera" based on a matrix of czechoslovak production MAB1256. The goal is processing of an interference image obtained in optical measurements.

Work is currently under way on a new module. Some semi-custom czechoslovak integrated circuits will be applied. The whole module is supposed to be constructed as one plug-in board for PC - XT(AT). At the same time work on the advancement of software is in progress.

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[3] NEC μPD7220A Graphics Display Controller. NEC Electronics (Europe). 1985.

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