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READOUT ELECTRONICS FOR THE π-e EXPERIMENT AT 50 GEV

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I. Introduction

The readout electronics for the $\pi - e$-experiment [1] controls the operation of the experimental setup, digitizes data from the detectors and transfers them to the computer.

The main logic diagram is presented in Fig. 1. The apparatus is synchronized with the accelerator and connected with the computer. A regime of the work is chosen by the operators.

The permission for triggering is given when the computer is set on-line and a gate signal comes from the control circuit. The trigger is produced by the system of scintillation counters and fast electronics during permission time.

Data from experimental setup pass the gates and are acquired only in the case of the trigger. Stored information is transferred to the computer through the output gates and the data bus.

The sources of information are as follows:

12 spark chambers (250 x 250 mm^2),

6 spark chambers (400 x 600 mm^2),

2 proportional chambers (80 wires),

about 20 scintillation counters (30 photomultipliers),

2 lead glass Cerenkov counters,

power supplies (for the counters, magnets, etc.).

The acquisition and on-line analysis is done by the HP 2116B computer with the parameters /2/:

word length - 16 bit,
cycle - 1.6 μsec,
memory - 32 k + 182 k (disk),
maximum transfer speed - 263 k/sec.

II. Main Units of the Readout Electronics.

1. Readout Electronics for Spark Chambers

In the experiment magnetostrictive spark chambers are used. For these chambers coordinates are given by time interval measurements between the trigger (or another zero time) and pulses from the magnetostrictive wire which corresponds to a spark in the chamber.

In Fig. 2 the preamplifier and amplifier-discriminator are shown. These circuits play an important role shaping the signals from pick-up coils into standard logic pulses. A signal from a pick-up coil is amplified 7 - 10 x 10^3 times and passes through the discriminator (T_1) which cuts noise and reflections. The output pulse corresponds to the maximum of the input signal (it is differentiated on the C_5 capacitor) or its leading edge (in this case a signal from T_1 goes to T_3).

The readout electronics contains 50 preamplifiers and amplifiers-discriminators.

For measurements the coordinates from the spark chambers, a parallel-series system based on magnetostrictive delay lines is used /3,4/. Compared with a parallel readout system /5/ this method gives a big advantage in the amount of electronics needed, but at the same time extends the measuring time, complicates logic and gives a little less accuracy and space resolution.

The block diagram of the spark chamber readout electronics is shown in Fig. 3. The signals from the amplifiers-discriminators

pass through the gates and are stored in the magnetostrictive delay line system [6]. The delay line used contains a few write coils along the wire and one read coil - this solution gives the possibility to store data with high density. The chain of the pulses from the delay lines is fed to a multiple position switch, which produces signals on the separate outputs. The width of these pulses corresponds to the arrival time of the input signals and they open the scalar gates for 20 MHz quartz clock. The count accumulated by the scalars gives coordinates of the sparks in the chamber. These values are sent to the computer.

The multiple position switch, gates and scalers are controlled by a circuit, which from the chain of the pulses separates only one spark chamber signals. After reset, the multiple position switch and the scalers are used for the data from the next chamber - this cycle is repeated many times.

The readout electronics contains two parallel channels for storage and measurements of the X and Y coordinates. Each channel has delay lines of the common length 2.4 msec, a multiple position switch and 12 scalers each of the 2^{14} capacity.

A more detailed description of the logic of this system will be given later.

2. Readout Electronics for the Proportional Chambers

For data from the proportional chambers [7], an 80 - channel, gated flip-flop memory is used. The block diagram of one channel is presented in Fig. 4.

A signal from a wire is amplified about 200 times, shaped to a standard amplitude and differentiated to the 50 nsec width. Such signals pass through the gates, which are opened for chosen time (typically 100 nsec) and are stored in the memory. The state of the memory is transferred to the computer.

3. Readout Electronics for the Scintillation and Lead Glass Cerenkov Counters.

Signals from the scintillation and lead glass Cerenkov counters are processed by fast electronics. The readout electronics gives a possibility to count pulses from the fast logic and latche signals from each counter.

Fig. 5. presents the block-diagram of one counting channel. Input signals pass through the gate controlled by the main control circuit. The accumulators count till or after the trigger, and their state is sent to the computer by each trigger.

The readout electronics contains 16 20 *MHz* accumulators each of the 2^{14} capacity.

The block diagram of one latche channel /8/ is shown in Fig. 6. The pulses from the fast discriminators come to the gate which is opened by the trigger for 20 nsec. The output pulses are stored in the flip-flop memory and their state is transferred to the computer by each trigger.

4. Voltage Measuring System.

Fig. 7 shows block diagram of the voltage measuring system. The scanner works synchronously with the accelerator cycle and using relays sends a voltage to the DVM /9/. The DVM is triggered extremely one time per accelerator cycle. The state of the DVM is transferred to the computer in each event.

The circuit periodically scans 32 test points.

5. Fixed Data Circuit.

For marking different regimes of the experimental set-up sixteen 10-position switches are used. The state of each switch is transferred to the computer in the BDC code.

III. Readout Electronics Control Logic.

1. The Synchronization with the Accelerator and the Computer.

In Fig. 8. the block diagram of the readout electronics is presented and in Fig. 9. the sufficient time diagram for one accelerator cycle is shown.

The pulse ACCELERATOR comes from the accelerator timing system and initiates the MASTER CONTROL unit which sends an INTERPUT signal to the computer. The arrival time of this pulse is adjusted so that is enough to switch the computer into the DIRECT MEMORY ACCESS mode before the spill. When the computer is ready it gives an ENABLE pulse which turns on a READY flip-flop in the readout electronics - this level is one of those necessary for trigger permission.

After interrupting, the control system reserves MONITOR TIME for MONITOR TRIGGERS, which can be produced by the external or internal generator. From the point of view of the readout system these triggers are the same as real ones but they generate test information : The counters are excited by light diodes and the chain of pulses at a fixed distance is fed to the coordinate measuring system.

Later on the control unit shapes a BEAM GATE signal, which is also necessary for producing permission for the trigger.

As the readout electronic can be triggered just before the end of the BEAM GATE, the SPILL TIME for the computer is delayed by SPILL END DELAY for 10 msec. After that a CLEAR TRIGGER is sent to the readout electronics, and the data accumulated by the end of the gate, are transferred to the computer. This trigger is only accepted by the computer when there is no overlap with the real trigger. It is also needed by the computer control system when there are no monitor and real triggers - the regime of the computer is changed for an on-line analysis only after two "magic", complementary words, used for format checking.

READOUT RESET DELAY extends READOUT ENABLE for an additional 10 msec and only after that the whole system is disabled untill the next spill.

2. Acquisition and Data Transfer.

Fig. 10. presents the time diagram of the readout electronics in the case of the trigger.

The GATE for the trigger is produced by the DEAD TIME unit when the following conditions are satisfied;

- READY is set by the computer ENABLE,
- BEAM GATE is on,
- DEAD TIME is off (there was no trigger in selected time),
- CLEARING FIELD is off,
- RESET is on (it means that the previous event is finished).

The TRIGGER fires the spark chamber HV pulsers, opens the gates for the PROPORTIONAL CHAMBERS and the LATCHES, stops (or starts) the ACCUMULATORS. The DEAD TIME unit produces the timing signal - DEAD TIME, the control circuits accept a RESET level and the pulsed CLEARING FIELD is turned on after 0.5 msec delay.

The TRIGGER sets into the operation of the spark chamber coordinate measuring system which composes the main part of the readout electronics - Fig. 11. shows the sufficient time diagrams.

The STROBE signal allows the AMPLIFIER output pulses to pass the DELAY LINES where the logic pulse START is also stored. It comes 3 - 5 μsec earlier than the first FIDUTIAL and is used by the control circuit for synchronization, especially, when there is no data from the chamber. In the case of checking this input is used for the chain of TEST pulses.

To speed up the acquisition process, the coordinate measuring and transfer circuits are organized in the "ping-pong" way. Each of the channels for the X and Y coordinates is divided into two identical parts X', X'' and Y', Y'', from which X', Y' digitize data first and then X'', Y'', when X', Y' are busy with data transfer. The control circuits, alternately, change the regime untill finishing data from all the chambers.

The information from the delay lines comes in the burst, the length of which is 60 μsec for the 250 x 250 mm^2 chambers and 130 μsec for the 400 x 600 mm^2 chambers. The distance between the beginnings of the bursts is 80 and 160 μsec.

The regime of the subchannels is controlled by the REGIME circuit and changes either 70 or 150 μ sec after the first pulse of the burst for the "small" or "large" chambers, respectively. The number of the chambers is known earlier and sufficient jumpers are set in the circuit. At the moment of the change, the REGIME RESET resets the 6 SPARK SWITCH, and the SCALER RESET resets these scalers (2^{14}), data from which were sent to the computer (they will be used for digitisation).

The readout system is constructed for a maximum of 6 sparks from one pick-up coil. The multiple position switch starts with the first FIDUTIAL. All the outputs are switched into the high level state, and the scalers start to count at the 20 MHz clock frequency. The pulses from the chambers successivly turn off the outputs and stop the scalers.

The readout logic is organized so that the information from a selected part of the system occurs on the DATA BUS line when there is a coincidence between the "group" signal (CHAMBERS, ACCUMULATORS, PROPORTIONAL CHAMBERS, FIXED DATA) and the "word" signal. The "group" signal comes from the READOUT unit with respect to the number of words transferred to the computer (a special scaler counts them) - data are transferred in the fixed format. The "word" signals are given from a 12 - position ring counter and they are wired in parallel to all groups. At the moment of the regime chamge the first READOUT signal is generated and information from the first X scaler (which is in the transfer regime) comes to the DATA BUS. The FLAG signal for the MICROCIRCUIT INTERFACE, which controls the acquisition of the data by the computer, is set after 0.5μsec delay. After storage of the data in the memory, the computer sends an ENABLE pulse to the readout electronics. It shifts the ring counter to the next position, the second

READOUT reads from the next scaler and the next FLAG goes to the computer. When the data from the X scalers are transferred, the some process is repeated for the Y coordinate scalers. The transfer time for 12 words is about 50 μsec.

During that time a new fraction of the data is stored in the X and Y subchannels, so the next regime change starts to read this information and prepares the scalers for a new digitizing process.

The readout system allows to measure the coordinates of six sparks from 38 "small" and 12 "large" chamber pick-up coils. It consists of 300 computer words.

When the acquisition of the data from the spark chambers is completed the READOUT unit transfers the information of the remaining groups: ACCUMULATORS, PROPORTIONAL, CHAMBERS, FIXED DATA (it includes the information from LATCHES and DVM), each of which consists of 12 words. After 336 words an event is completed (Fig. 12), and the computer sends a CLEAR pulse to the readout electronics. This pulse finishes the work of the READOUT unit, resets all the systems by a RESET and turns off the READY level - it is restored by the next ENABLE signal which comes after the storage of the event.

If all the conditions for the GATE are satisfied the next trigger is possible.

IV. Some Technical Data

1. Construction

The readout electronics has been mounted in one "Vishnya" rack in 160 x 160 mm^2 and 80 x 160 mm^2 modules.

The rack is supplied by 220 V 50 Hz. The electronic circuits are supplied by 12 V "Aleksandryt" power supplies and 3V 5A and 6V 5A power supplies which we have constructed in 160 x 160 mm^2 modules. The system has a monitor circuit for checking the power supplies. It indicates the changes greater than 5%.

The readout electronics contains a similar unit which makes it possible to check all the control circuit without the accelerator or computer.

As a way of visual checking the information transferred to the computer, an indicator circuit has been built. It is possible to stop the transfer at any selected word.

The integrated circuits mounted on the double side printed boards were used for most of the circuits we had designed.

2. Exploatation.

The readout electronics has worked in the experiment for more than one thousand hours.

The following parameters have been obtained:

- accuracy of the track localization in the spark chamber - $\pm$ (0.2 - 0.4) mm,
- space resolution for one pick-up coil - about 5 mm,
- counting speed of the accumulators - 20 *MHz* ,
- time resolution of the proportional chambers - $2\tau \geq 80$ nsec for efficiency close to 100%.
- time resolution of the latches - 20 nsec.

V. Acknowledgements

In the construction, mounting, adjustments and exploatation of the readout electronics a large team of physicists, engineers and technicians has participated.

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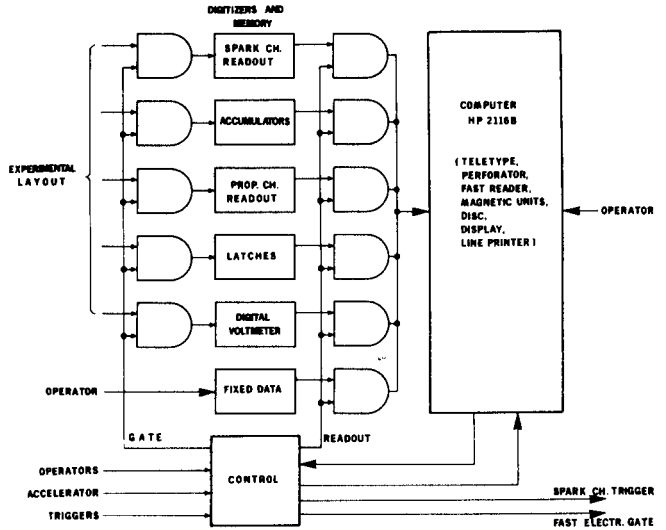


Fig. 1. Main logic diagram.

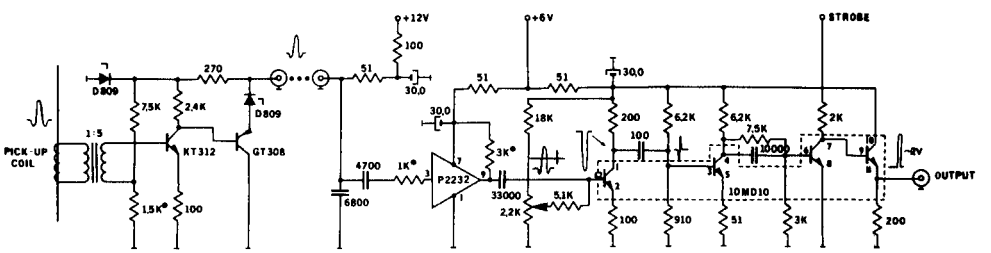
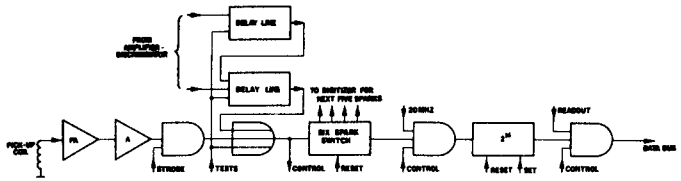
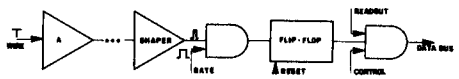


Fig. 2. Preamplifier and amplifier discriminators for the spark chambers.



g. 3. Block diagram of the electronics for the spark chambers.



ig. 4. Block diagram of the electronics for the proportional chambers.

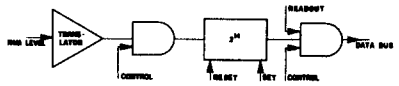


Fig. 5. Block diagram of the accumulator.

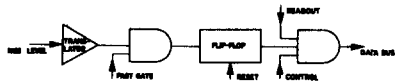


Fig. 6. Block diagram of the latches.

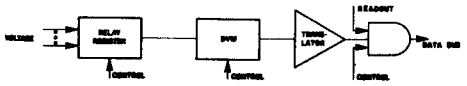


Fig. 7. Block diagram of the DVM scanner.

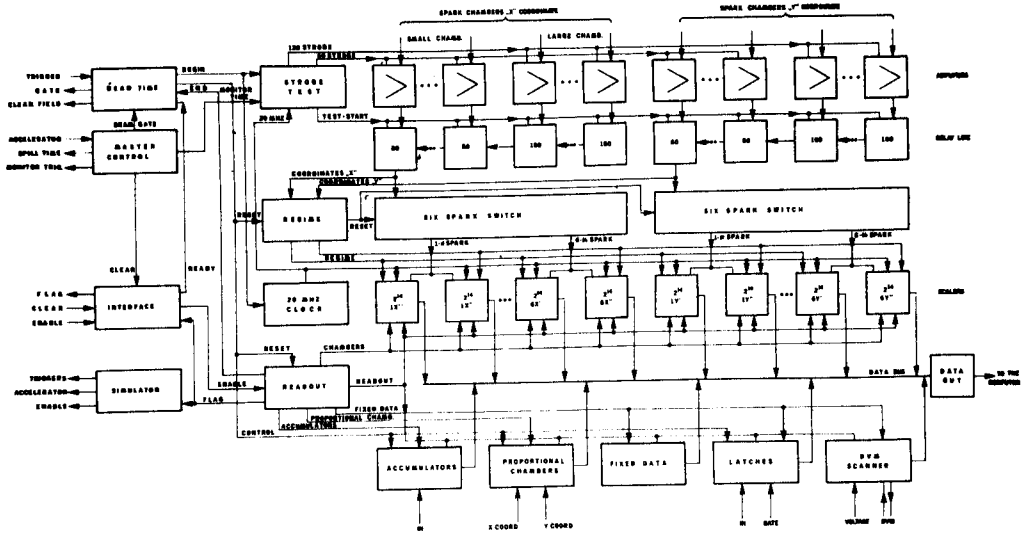


Fig. 8. Block diagram of the readout electronics system.

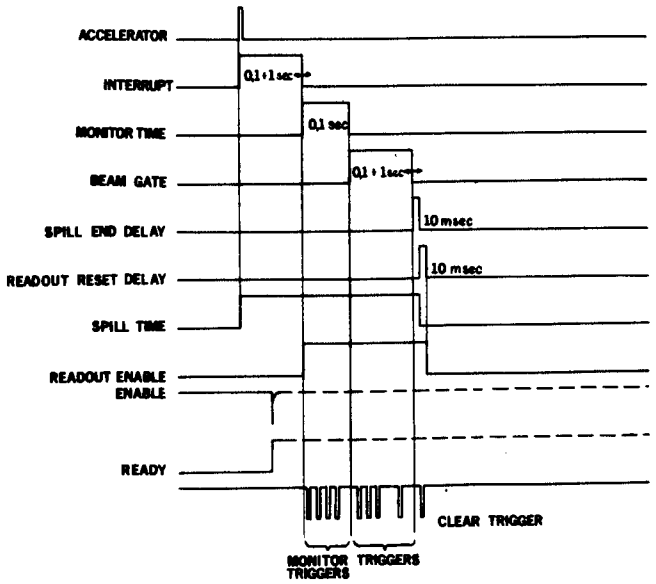


Fig. 9. Time diagram of the readout electronics for one accelerator cycle.

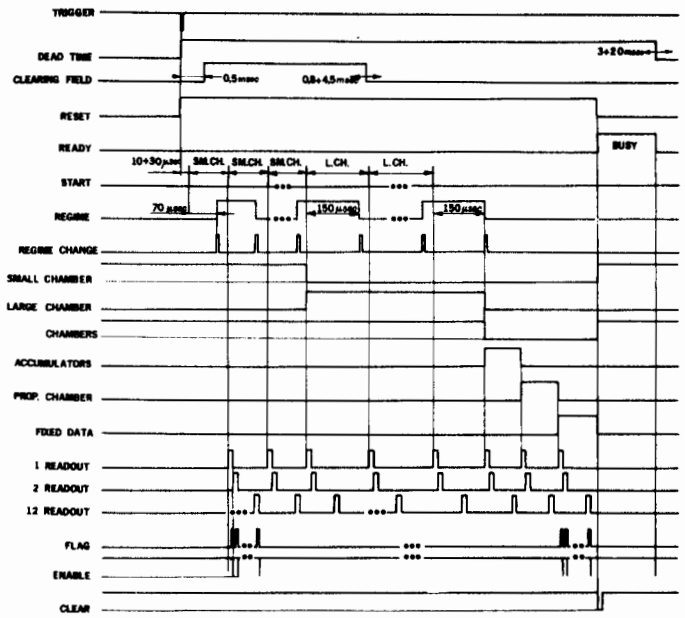


Fig. 10. Time diagram of the readout electronics for one trigger.

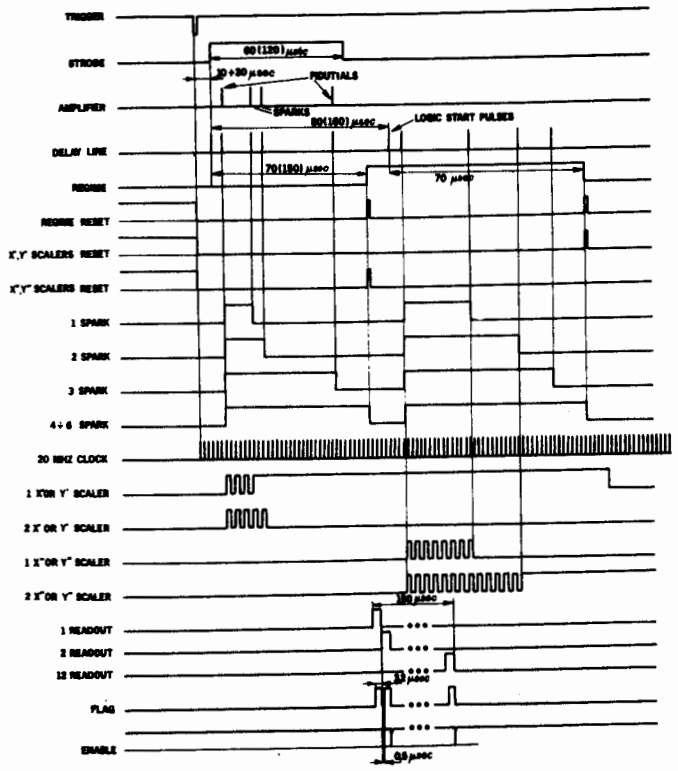


Fig. 11. Time diagram of the spark chamber coordinate measuring system.

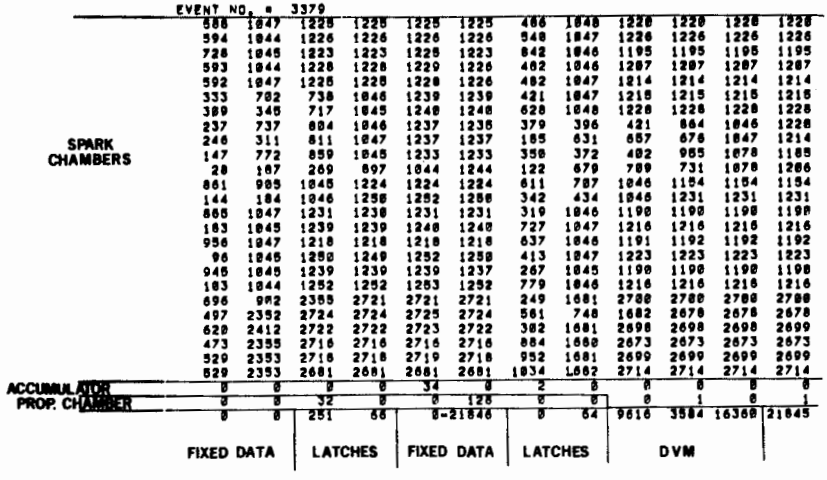


Fig. 12. One physical event format.