ОБЪЕДИНЕННЫЙ ИНСТИТУТ ЯДЕРНЫХ ИССЛЕДОВАНИЙ
ЛАБОРАТОРИЯ ЯДЕРНЫХ ПРОБЛЕМ

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FERRITE-CORE INTERMEDIATE MEMORY FOR HANDLING INFORMATION PRESENTED BY RADIATION DETECTOR SYSTEMS

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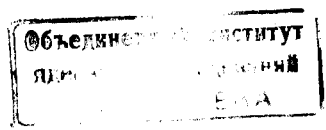

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1. Introduction

During the automatic nuclear physics experiments, generally, the information given by the radiation detectors is transmitted onto a digital information handling line to get results in a form which manifests the qualitative or quantitative characteristics of the physical events. These information handling lines in most of the cases include an intermediate memory to give a match between two parts of the line with respect to the time and the number of bits.

The intermediate memory which is the subject of our present discussions has been intended to transfer information presented by a number of scintillation detectors of a spark chamber experiment onto a punched paper tape. During its construction the possibility of a later more wide-ranging exploitation was taken into account.

The logical structure of the memory is accomodated to the synchrocyclotron of the Laboratory of Nuclear Problems of the Joint Institute for Nuclear Research in Dubna which has a burst time of 600 μ sec and a period of 10 msec.

2. System Considerations

In those cases when the event-rate is sufficiently low and the dead time of the accelerator is relatively long there is a possibility to separate the acquisition time of the information from the hand over time of it for the memory. So, the information received by the memory during the burst time can be transferred onto the punched paper tape during the dead time of the accelerator[1,2]. Under the circumstances of the given nuclear experiment such a time separation is not possible and therefore an interlaced memory system was chosen[3,4]. According to the operation conditions of such systems the given memory consists of a high-speed and of a low speed unit. The high-speed unit is ready to receive information from the measuring system during each burst time. On the other hand, the low-speed unit transfers information from the memory onto the punched paper tape continuously (during the burst time too) as long as the memory contains information.

To avoid disturbing action between the two parts of the memory an information transfer from the high-speed unit to the low-speed one is always performed in the accelerator-dead time.

3. General Description

3.1 High-speed unit

The block-diagram of the memory is given in Fig. 1. The basic part of the high-speed unit is the 120 (48 bit) word memory block.

The 48 bit information codes crossing a coincidence-gate system are first stored in a write-register and from there they will be transferred in the selected word-lines of the memory block.

The write (and read from the memory block) cycle is 8 μ sec.

If an event occurs in the measuring system, a preselection unit presents an event-pulse, which will be used as a write-command pulse (see WRITE-COMMAND input). If in the memory block there is at least one free word line the event pulse gets on the input of the 10 μ sec ONE-SHOT circuit. But if there is no empty word line in the block, the gate circuit L_1 (it is an AND-GATE with negation) will shut the way of this pulse. This state remains as long as, at least one word-line is emptied by a reading process.

The 10 μ sec ONE-SHOT generally closes the COINCIDENCE-GATE CIRCUITS. After receiving an event-pulse it gives a 1 μ sec gate pulse for the COINCIDENCE-GATE CIRCUITS, and opens them for that time. The information-code is translated into the WRITE-REGISTER in the opened state of these circuits. Simultaneously, the WORD-SELECTION SYSTEM AND CONTROL unit gets a command pulse too, and as a result, it selects a word-line and after it transfers the information-code from the WRITE-REGISTER into the selected word-line.

It is a characteristic feature of the ONE-SHOT, that after receiving an event-pulse for 10 μ sec all others will be rejected. In this way the possibility of disturbing a write-process in progress by an event pulse is excluded.

The reading of information from the memory block is carried out by the READ-COMMAND pulse. During the read cycle the information from the word line selected by the WORD-SELECTION SYSTEM AND CONTROL UNIT, runs over the GATED SENSE-AMPLIFIERS in the READ-REGISTER which is the basic part of the low-speed unit.

For the read command signal a pulse is used appearing in coincidence with the front of the burst. This pulse runs over 1. BISTABLE, the gate circuit-L_2 and the DELAY-CIRCUIT to the WORD-SELECTION SYSTEM AND CONTROL block with a delay more than the burst time. Thus, a read-process from the memory block can take place only during the dead time between the bursts.

The read-command pulses can affect the memory only in those cases, if

1) at least, in one word-line an information can be found and if,

2) the low-speed unit is free to accept information.

The fulfillment of the first condition will be indicated in such a way, that the gate- L_2 is opened if there is a stored information in the memory, but closed if it is empty.

The "free-state" of the low-speed unit is shown by the ZERO-state of the 1. BISTABLE.

The memory has two, independent from each other, address systems. One of them serves to determine the sequence of the write-address and the other one - the sequence of the read-addresses. The sequences are the same in both cases. For a read-process can be performed only then, if at least, one memory register holds information, the read-address system can follow and overtake but not proceed the write-address system. The filling state of the memory, that is the number of the word-lines occupied by information is registered by the DIFFERENTIAL SCALER [5]. This scaler counts the difference of the number of the write and read command pulses. If the value of this difference is zero, it shows that the memory block is empty. In this case the DIFFERENTIAL SCALER closes the gate - L_2. On the other hand, if the registered difference is 120, it indicates that all the word lines are occupied by information. If it is so, the DIFFERENTIAL SCALER will close the gate- L_1 preventing further write-processes.

3.2 The low-speed unit

The low-speed unit of the memory consists of the WRITE-REGISTER mentioned earlier, of the pulse current COMMUTATOR and its driver, of the free-running CLOCK-GENERATOR and of ancillary circuits with logical functions.

The task of the low-speed unit is to transfer the information stored in the READ-REGISTER into the perforator with a speed which satisfies the requirements concerning the perforator. The information arrives to the READ-REGISTER as a 48-bit parallel code, but as the punched paper tape has only 4 tracks to accept the information it will be sent to the perforator in 12 steps.

The low-speed unit is controlled also by the READ-COMMAND pulse. This signal has no time correlation with the clock-pulses. To avoid the problems which may arise about these conditions, a time correlation between these signals is established in the low-speed unit. To do this, the command-pulse after finishing a read cycle from the memory block first enters on a 1 bit memory circuit [6]. From here it can run to the input - 1 of the 2.BISTABLE only in coincidence with the next clock pulse. At this moment the 2.BISTABLE will be trig-

gered and it will open the gate- L_3 (AND-circuit). Now the path is free for the clock pulses to the COMMUTATOR-DRIVER. Under the influence of these pulses the information stored in the READ-REGISTER will be shifted to the perforator.

Each of the information blocks (words) is marked on a fifth track of the paper tape by one hole. The marker signals are produced in coincidence with the first step of the perforator.

During the operation of the low-speed unit the 1.BISTABLE occupies a ONE-state and it cannot accept further write-command pulses. In coincidence with the 12-th step of the commutator both this and the 2.BISTABLE return to the ZERO-state. With that the operation-cycle of the low-speed unit is closed and the memory is prepared to accept the next read-command pulse.

4. Circuit Details

4.1 The Memory-Block

The memory block is a linear selection (LSM), two core per bit system with current bias[7,8,9]. It includes 120 word-lines. The store capacity of a word-line is 48 bits. The word-transformers are built on square-loop ferrite cores. The 120 transformers are arranged in a three-dimensional system in such a way as it is shown in Fig. 2 with 8 transformers for simplicity. In spite of the three-dimensional system, the principle of the word selection by a coincidence of two half-selection currents was preserved.

The 120 transformers are arranged in 8 planes. Each of the planes contains 15 transformers. In the planes there are 5 transformers along the x-rows and 3 transformers along the y-columns.

The three-dimensional solution makes it possible to use a more economic word-selection system, than that of the two-dimensional one[10].

4.2 Word-Selection, Reading and Writing

The line of an addressed word can be selected by the aid of the coordinate windings belonging to the word-transformer of the addressed word, The windings themselves will be selected by the selection-switches and the latter - by the address-scalers.

According to the three-dimensional selection structure 5, 3 and 8 selection switches belong to the memory block in the x, y and z-directions, respectively. One of the coordinate windings of a word-transformer may be accessible by one of the S_z-switches, and the other one - by a pair of the (S_x, S_y) - switches. One of the switches S_z determines a plane of the array and a pair of the switches S_x and S_y - one of the z-directions.

The system of the selection switches is built on the basis of the current-steering principle[11,12]. "Closing" of a (S_x, S_y, S_z) triplet of the switches means that all the diodes of the coordinate windings get an inverse voltage except those of the selected ones.

On the basis of the block-diagram of the plane selection system (Fig. 3) a few details about the selection process can be cleared out. Consider, e.g., the selection of the 3-d coordinate winding (x-y plane 3) during a read cycle, which will be as follows:

Before the appearence of a read-command pulse the READ ADDRESS SCALER had already been prepared (by the latest read process) to select the switch of the plane-3. As a command-pulse (P_{cr}) arrives, the appropriate driver gives a pulse (P_r) for the READ ADDRESS SCALER. The scaler steers this pulse to the preset circuit of the switch - S_{z3}. By this pulse the switch will be selected. The time of selection is $t' < t_1$. After t_1, when the selection process is already finished, the delayed read-command signal starts the INTERROGATIVE DRIVER. It will be the pulse - P_i of this driver which closes the selected switch - S_{z3}. By closing this switch all the diodes of the coordinate-windings get an inverse voltage except that of the 3-d one. The switch on process is kept for a time $t'' < t_2$. After t_2 the read-command pulse will start the x-y PLANE CURRENT DRIVER, which sends a half-selection current across the 3-d coordinate winding.

The selection of a switch belonging to a z-derection coordinate winding marked by the x-y address-scalers and after it the supply of that winding by a half-selection current is carried out in a similar manner in coincidence with the plane-selection.

Now the word-transformer lying in the cross point of the half-selection currents switches and the information stored in its word-line will be read and transferred to the READ-REGISTER. For the transfer time the GATED SENSE-AMPLIFIERS (see Fig. 1) get a strobe pulse.

After finishing the read-process both the selected word-transformer and the selection switches return to their stationary state under the influence of a current bias.

A write process takes place in a similar manner. But during the pulses (P_{xy}, P_z) of the coordinate drivers the GATED SENSE-AMPLIFIERS do not get any gate-pulse and so this period of the write-cycle will be a simple clearing of the word-line. The write process itself will be performed in the word-transformer return period in coincidence with the operation of the bit-write system (see the next section).

The address scalers are ferrite-core ring-commutators [13] (see also in 4.4). According to the three-dimensional selection system there are three read- and three write-address scalers. The number of the stable states of the scalers are 5, 3 and 8 in the x, y, and z directions, respectively. Under the influence of a command pulse the address will be altered, in all the coordinate directions by +1. In this manner the sequencial of the word selection shows a zig-zag space pattern.

4.3 The WRITE-REGISTER and Bit-Write System

The WRITE-REGISTER and the bit-write system form a close unit. It is the peculiarity of this unit, that its primary bit-circuits include only passive components. The system with its preset drivers and coincidence gates is shown in Fig. 4 for the case of 4 bits.

The task of the primary bit circuits is double:

1) they preserve the information received from the measuring system, and

2) during the write-period they distribute the pulse current of a common bit driver among the single information windings of the memory block. The pulse polarity on the output of a single bit-circuit will be consistent with the binary digit stored in it.

The primary circuits are built on square-loop ferrite core elements and their operation is based on the current-steering principle.

If a ZERO was written into the primary circuit during the transfer of information (it did not receive any signal from the PRESET DRIVER) then during the write period the pulse current runs across the branch α. But where the primary circuit received a ONE-signal there during the write period the current will run across the branch β.

As the primary windings of the output pulse transformer-Tr have opposite polarities concerning the secondary one, the information write winding will get a current with a positive or negative polarity according to the write-ZERO or write-ONE as it is necessary by the two-core per bit systems.

Each write-cycle is closed by a reset period when all the primary circuits return to the ZERO-state under the influence of the RESET DRIVER.

The timing cart of the read and write cycle is shown in Fig. 5. As is seen, the course of both processes are the same. But for the write process there will be used always the second part of the word-line pulse and for the read-process - the first part of it. In Fig. 5 is shown the word-line pulse together with its mirror reflection. $P'_{\text{word line}}$ refers to the first and $P''_{\text{word line}}$ to the second memory core of the two core per bit cells.

4.4 The Read-Register and the Commutator

The READ-REGISTER [14] consists of 48 square-loop ferrite cores according to the number of bits of a word. The cores are set in a (12x4) matrix array as it is shown in Fig. 5. Before transferring information into the register all the cores can be found in the ZERO-state. During the transcription of a code from the memory block into the register every core which finds a ONE in the code will be switched into the ONE-state.

By reading the register the commutator will steer the pulses of the commutator driver in a sequence on the interrogative wires 1,2, ..., 12 of the matrix. Thus the code will be transferred from the register into the perforator in 12 steps (at every step of 4 bits) across the read-wires of the matrix and the perforator drivers.

The commutator [13] is also a current steering system built on square-loop ferrite cores. The ferrite elements are arranged in two rows. In the stationary state the cores of the upper row are in the ZERO-state except that of the branch selected for the next commutator cycle. The cores of the lower row are held in the ZERO-state by a bias current.

In the first period of the commutator cycle the elements of the upper row will carry out a transition ZERO-to-ONE in such a way, that all the diodes of the current branches will get an inverse voltage except that of the selected one. As a consequence, the current of the pulse source connected to the points $\alpha - \beta$ will run across the selected branch. At the same time one of the ferrite core elements of the lower row will be switched, too. In the second period of the commutator cycle, all the cores which are in the ONE-state trend to return to the ZERO-state. But one of the core elements of the upper row cannot be transferred to the ZERO-state because it gets an inhibit current from the reswitching element of the lower row. The inhibit circuit includes two diodes. One of them is a common switching type and the other one is a Zener-diode. The polarity of the diodes and the windings and the number of turns are chosen in such a way that an energy transfer is possible only from below upwards.

5. Additional Remarks

The operation of the memory is tested by a built-in control system [10] which presents determined codes for the input, and supervises the output answer with logical check circuits. There is a possibility to control the pulse forms in the sufficient point of the memory by a built-in oscilloscope.

The input resolution time of the memory determined by the ONE-SHOT is 10 μ sec. Taking this and the word capacity of the memory into account, one can see that the maximum rate of the events handled by the system is bounded by the perforators being at disposal at the present time. The application of a high-speed magnetic tape recorder, if necessary, encounters no difficulties.

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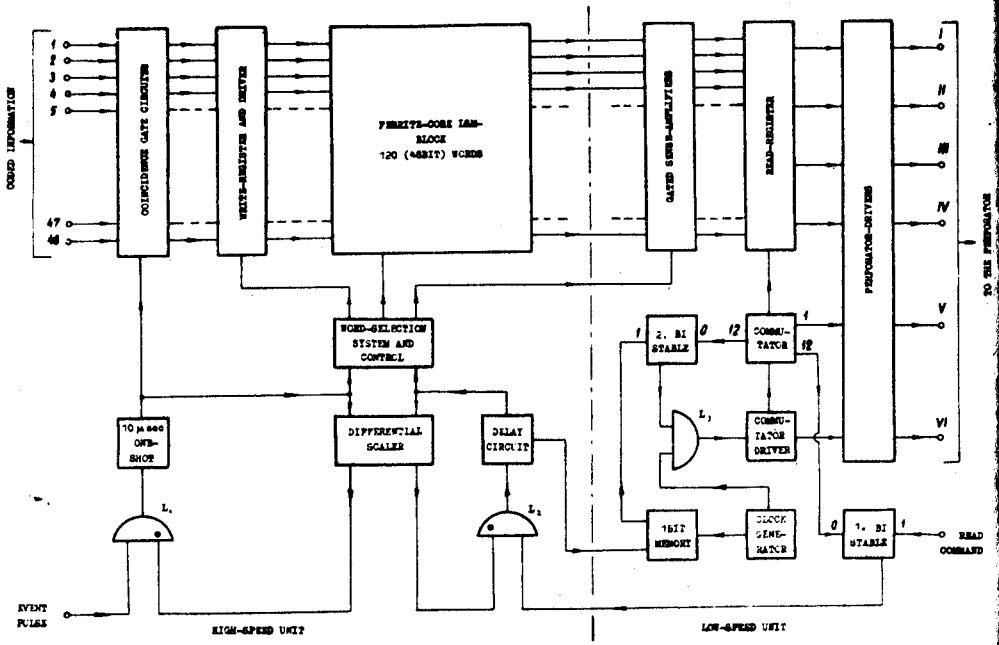
CODED INFORMATION
1
2
3
4
5
47
48
COINCIDENCE GATE CIRCUITS
WRITE-REGISTER AND DRIVER
FERRITE-CORE MEMORY BLOCK
120 (48BIT) WORDS
GATED SENSE-AMPLIFIERS
READ-REGISTER
PERFORATOR-DRIVERS
I
II
III
IV
V
VI
TO THE PERFORATOR
WORD-SELECTION SYSTEM AND CONTROL
2. BI STABLE
COMMUTATOR
COMMUTATOR DRIVER
10 μ sec ONE-SHOT
DIFFERENTIAL SCALER
DELAY CIRCUIT
16BIT MEMORY
BLOCK GENERATOR
1. BI STABLE
READ COMMAND
EVENT PULSE
HIGH-SPEED UNIT
LOW-SPEED UNIT

Fig. 1.

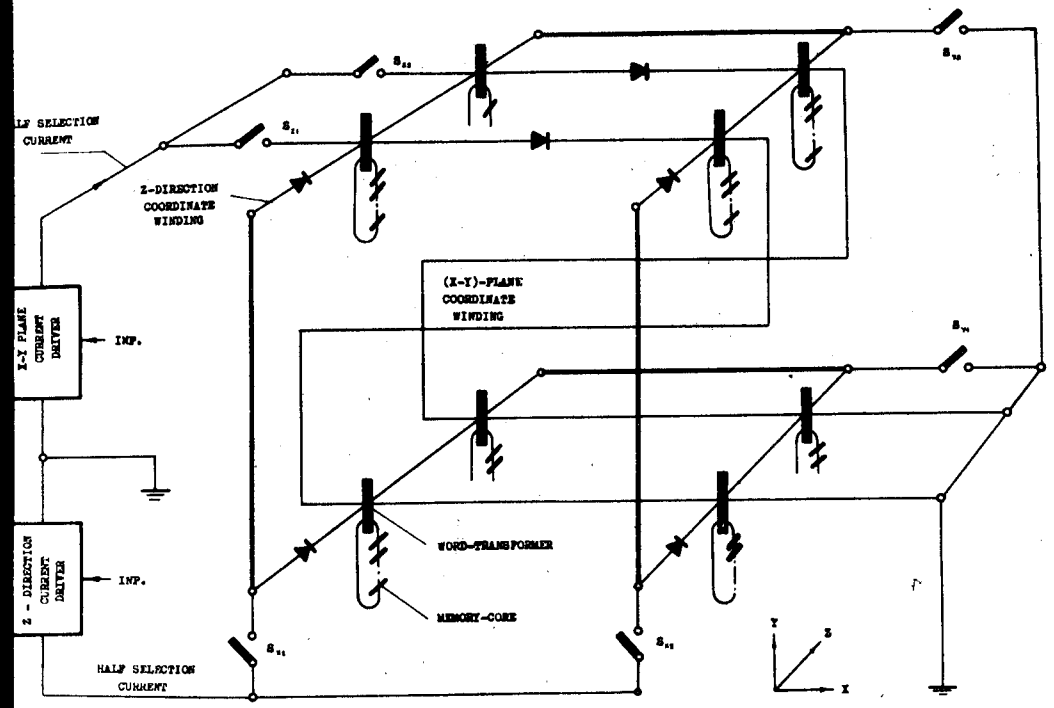
HALF SELECTION CURRENT
Z-DIRECTION COORDINATE WINDING
(X-Y)-PLANE COORDINATE WINDING
X-Y PLANE CURRENT DRIVER
INP.
Z - DIRECTION CURRENT DRIVER
INP.
WORD-TRANSFORMER
MEMORY-CORE
HALF SELECTION CURRENT
Y
Z
X

Fig. 2.

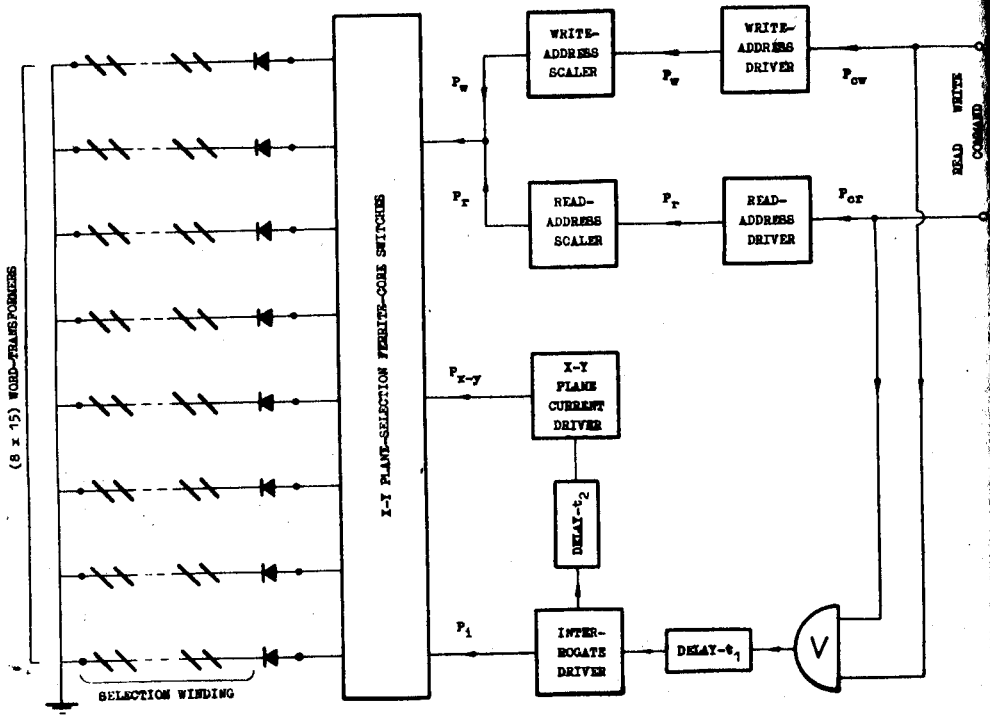
(8 x 15) WORD-PHASE-POWERS
X-Y PLANE-SELECTION FERRITE-CORE SWITCHES
WRITE-ADDRESS SCALER
WRITE-ADDRESS DRIVER
READ-ADDRESS SCALER
READ-ADDRESS DRIVER
X-Y PLANE CURRENT DRIVER
DELAY-t_2
INTER-ROGATE DRIVER
DELAY-t_1
V
READ WRITE COMMAND
SELECTION WINDING

Fig. 3.

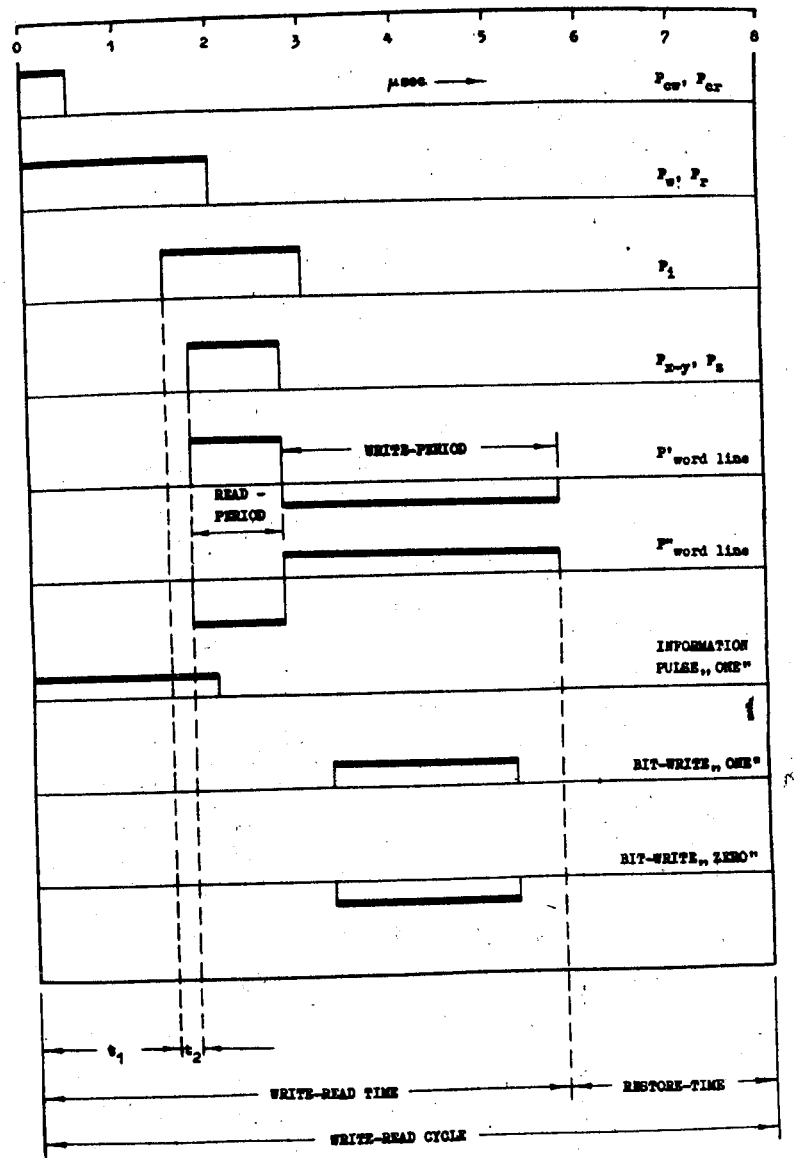
0 1 2 3 4 5 6 7 8
μsec.
WRITE-PERIOD
READ-PERIOD
word line
word line
INFORMATION PULSE „ONE"
BIT-WRITE „ONE"
BIT-WRITE „ZERO"
WRITE-READ TIME
RESTORE-TIME
WRITE-READ CYCLE

Fig. 4.

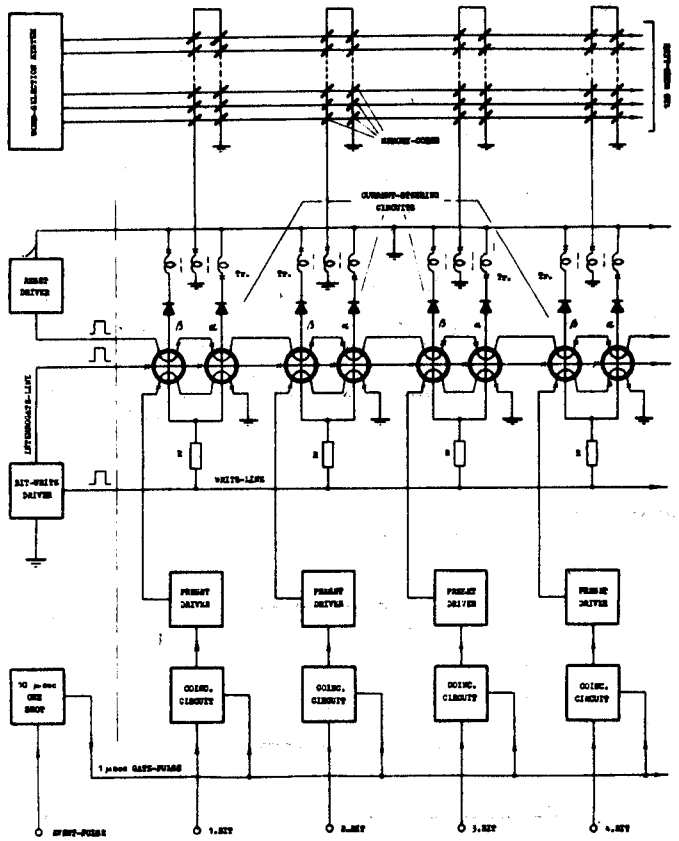

Fig. 5.

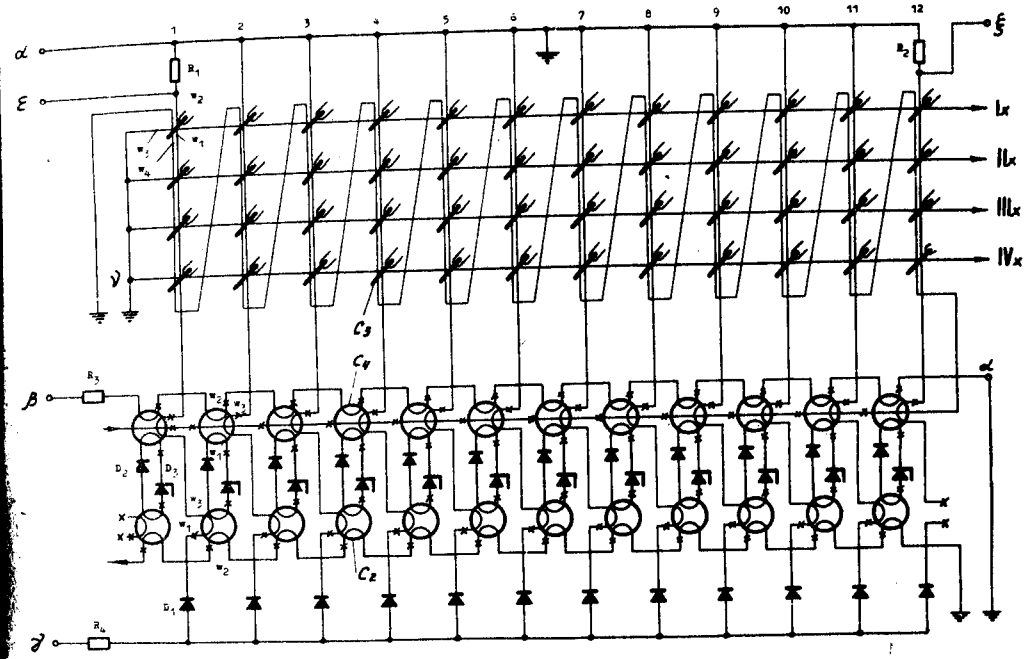

Fig. 6.